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# **Towards single nanowire solar cell based on novel radial p-n junction**

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<p>One of the most promising applications, the 1D semiconductor nanowires (NWs) offer, is the development of next generation solar cells at low-cost and higher efficiency. Group III-V semiconductor NWs, especially GaAs and InP, are the ideal semiconductor materials to build such devices on low-cost platforms. The aim of this work was to fabricate and study the fundamental working mechanisms of single nanowire solar cell and photodetector based on novel radial p-n junction in a core-shell geometry. The Au-assisted GaAs NWs were grown and doped in situ using metalorganic vapour phase epitaxy (MOVPE). In this study, a unique lithography-free technique was employed on an ensemble of NWs to isolate the core (p-type) from the shell (n-type) on the growth substrate. Electron beam lithography (EBL) was used to make metal contacts to the single core-shell NWs. In that respect, specific contact schemes were developed to realize ohmic contacts between the metal electrodes and the NWs. Electrical measurements of single nanowire device revealed perfect I-V behaviour confirming the formation of radial p-n junction diode. For characterization of NWs, scanning electron microscopy (SEM), transmission electron microscopy (TEM), photoluminescence (PL) and photocurrent spectroscopies were employed.</p> <p>Surface passivation of NWs was identified as one of the key issues in functioning of the photovoltaic device as no photo response was detected without the same. The surface passivation of GaAs NWs with higher band gap AlGaAs layers resulted in dramatic enhancement of the PL intensity, and the photocurrent measurements of the device revealed a broad photo response in the visible spectrum range, indicating a successful working of a single nanowire as a photodetector. However, although a functioning radial p-n junction was demonstrated, no solar response was detected from the single nanowire structure because of yet many unaddressed challenges such as high contact resistance, doping optimisation, absence of intrinsic region and unoptimised geometry. In summary, a single nanowire based photodetector was successfully demonstrated, and a full fabrication process was studied and developed for making progress towards realising the functional single nanowire based radial p-n junction solar cells in the future.</p>			
<b>Keywords:</b>	nanowire, metalorganic vapour phase epitaxy, photodetector, solar cell, core-shell, p-n junction		
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# Preface

I would like to thank my supervisor Professor Harri Lipsanen for the opportunity to make my thesis in his group at the Department of Electronics and Nanoengineering of Aalto University. He opened the world of nanoscience to me and encouraged me to explore it ever since.

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# Abbreviations and Acronyms

ALD	Atomic layer deposition
BSE	Backscattered electrons
CBE	Chemical beam epitaxy
CVD	Chemical vapour deposition
CS	Core-shell
DEZn	Diethylzinc
EBL	Electron beam lithography
EDX	Energy-dispersive X-ray spectroscopy
FCC	Face-centered cubic crystal structure
FET	Field-effect transistor
HF	Hydrofluoric acid
HV	High vacuum
IPA	Isopropanol
I-V	Current-voltage
LED	Light-emitting diode
MBE	Molecular beam epitaxy
MFC	Mass flow controller
MIBK	Methyl isobutyl ketone
MMA	Methyl methacrylate
MOVPE	Metalorganic vapour phase epitaxy
NP	Nanoparticle
NW	Nanowire
PCE	Power conversion efficiency
PE	Primary electrons
PL	Photoluminescence
PLL	Poly-L-Lysine
PMMA	Polymethyl methacrylate
PVD	Physical vapour deposition
RIE	Reactive ion etching
RT	Room temperature (300 K)

SCCM	Standard cubic centimeters per minute
SE	Secondary electrons
SEM	Scanning electron microscope
Si <sub>2</sub> H <sub>6</sub>	Disilane
SiN <sub>x</sub>	Silicon nitride
SiO <sub>2</sub>	Silicon dioxide
SOG	Spin-on glass
SRV	Surface recombination velocity
TBA <sub>s</sub>	Tertiarybutylarsine
TBP	Tertiarybutylphosphine
TCO	Transparent conductive oxide
TEM	Transmission electron microscope
TESn	Tetraethyltin
TMAI	Trimethylaluminum
TMGa	Trimethylgallium
TMIn	Trimethylindium
UHV	Ultra-high vacuum
VLS	Vapour-liquid-solid
WZ	Wurtzite crystal structure
ZB	Zinc blende crystal structure

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# Chapter 1

## Introduction

According to International Energy Agency, in 2014 human civilization produced 159 319 TW h of energy which is 224% more than in 1973. The most significant amount of energy was supplied with conventional energy sources such as oil, gas and coal that accounted for more than 81%. A striking point is that only 14.1% of energy in 2014 was produced with renewable energy sources including a tiny fraction of 1.4% that was supplied by geothermal, wind and solar energy. Besides the fact that conventional sources are depleting rapidly, the effect that fossil fuels burning has on the climate and the environment is clearly poisonous and irreversible. At the same time, Sun irradiates the Earth's surface with about 120 000 TW h every hour which is more than the world's yearly energy consumption (109 612 TW h in 2014). [1] Although the photovoltaics industry is progressing rapidly with average growth rate of 49% per year (cumulative installed capacity), its contribution to the total energy production worldwide is still negligible. [2] This is mostly due to the cost of kWh of solar energy which is currently higher than of the conventional fossil fuels. Furthermore, the average efficiency of commercial silicon solar cell was 16% in 2013 and it is growing only by 0.3% annually. Apparently, there is a strong demand for cost reduction, lower material usage and higher conversion efficiency of the photovoltaic modules. The use of III-V semiconductor nanowires for fabrication of the next generation solar cells can overcome these issues and push forward the photovoltaics industry.

A nanowire (NW) is a special one-dimensional (1D) nanostructure that usually has a diameter less than 100 nm and typical length of several micrometres. NWs are often referred to as one-dimensional structures as they have extremely high surface-to-volume ratios due to mostly elongated surface along the nanowire body. NWs have been a subject of intensive research over the last decade as they offer a lot of interesting mechanical, electrical and optical properties that make them potentially useful for a variety of applica-

tions including photonics, optoelectronics and novel solar cells. [3] Due to the unique properties (direct band gap, high carrier mobility) and dimensions on the scale of visible light wavelengths, NWs allow superior light absorption and charge collection as they practically act as light concentrators. Integration of NWs on lattice mismatched Si substrates and even cheap glass substrates allows to dramatically cut materials costs and achieve superior conversion efficiencies.

The aim of this work was to fabricate and study the fundamental working mechanisms of single nanowire solar cell and photodetector based on novel radial p-n junction in a core-shell geometry. This thesis is divided into six chapters. Following the introduction, the theory behind III-V semiconductors is discussed in chapter 2. Chapter 3 reviews the crucial aspects of semiconductor NWs such as synthesis mechanisms, effects of the growth conditions and doping. In addition, NW based devices and applications are reviewed with the focus on NW solar cells. Chapter 4 presents the equipment that was used in this work and the main operational principles. The obtained results, characterization data as well as thorough description of the whole fabrication process are described in chapter 5. Finally, conclusions are drawn in chapter 6.

## Chapter 2

# Theory of III-V semiconductors

This chapter presents the fundamental theory behind III-V semiconductors. Sections 2.1-2.3 focus on the concepts of electronic band structure and crystallography. III-V compound semiconductors are presented in section 2.4. Section 2.5 describes intrinsic and extrinsic semiconductors and section 2.6 gives overview of the p-n junction as a basic building block of almost any electronic device.

### 2.1 Crystal structure

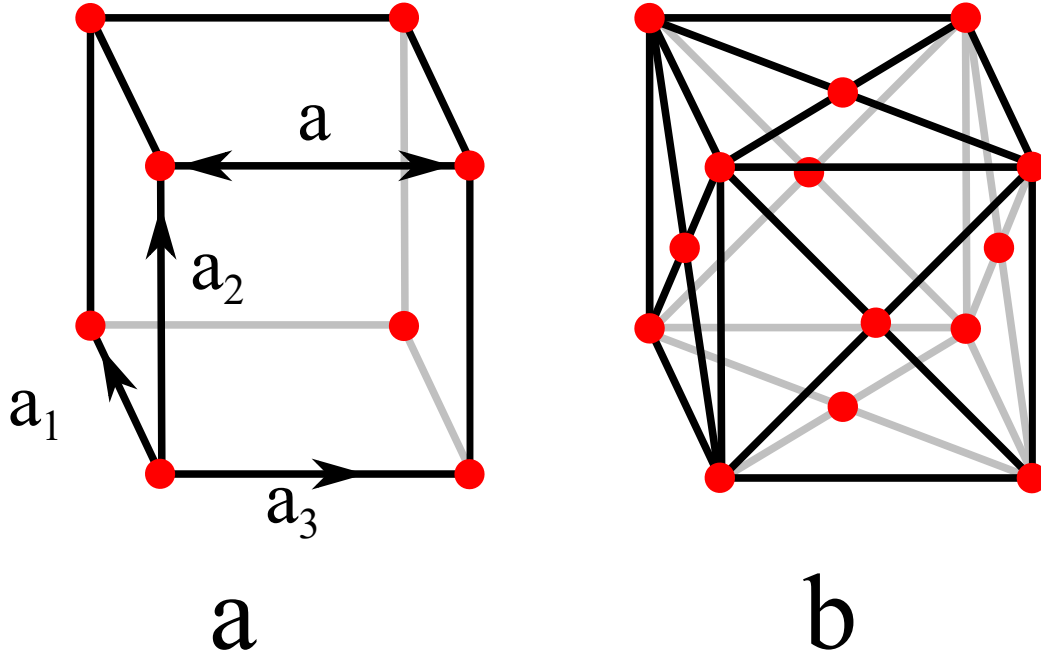
Most of the solid and semiconductor materials have crystalline structure meaning that their atoms are arranged in a certain ordered and repeated manner. This is also true for group III-V semiconductors that are synthesized epitaxially. Crystal structure of every crystal can be described in terms of crystal lattice and basis. Crystal lattice is an abstract concept that defines a discrete but infinite set of points in space that form a periodic structure. Basis is a group of atoms that is repeatedly attached to each lattice point effectively forming a crystal structure. Lattice can be specified using primitive vectors  $a_1$ ,  $a_2$  and  $a_3$  and every lattice point  $R'$  can be derived from another point  $R$  as

$$R' = R + m_1a_1 + m_2a_2 + m_3a_3 \quad (2.1)$$

where  $m_1$ ,  $m_2$  and  $m_3$  are fractional coordinates. By combining all possible combinations of  $m_i$ , entire crystal structure can be formed. The smallest volume confined by primitive vectors is called primitive unit cell. [4, p. 3-4] Figure 2.1 (a) shows a simple cubic lattice which is one the most common and simple primitive unit cells. It has four lattice points that represent atoms.



Each atom is equally shared between adjacent unit cells and, therefore, primitive cubic unit cell contains one atom in total.

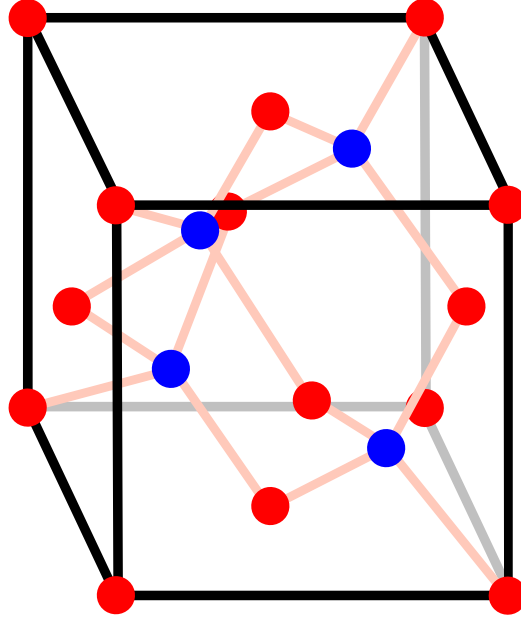


**Figure 2.1:** Schematic diagram of (a) primitive cubic unit cell and (b) face-centered cubic (FCC) unit cell. Primitive cubic lattice is enclosed by primitive vectors  $a_1$ ,  $a_2$  and  $a_3$ . Corners of the cube are lattice points that represent atoms. Lines represent bonds. Lattice constant  $a$  is either length, width or height of the cube and it signifies the physical dimension of the primitive unit cell. Face-centered cubic unit cell has additional atom at each face of the cube.

Figure 2.1 (b) depicts face-centered cubic (FCC) lattice that additionally has one atom at each face of the cube resulting in total four atoms per unit cell. The bulk crystal can be formed by repeating the unit cell in all directions. The cube's edge length is denoted by  $a$  and it is called lattice constant. Lattice constant defines the physical dimension of the primitive unit cell and it is different for different material compositions.

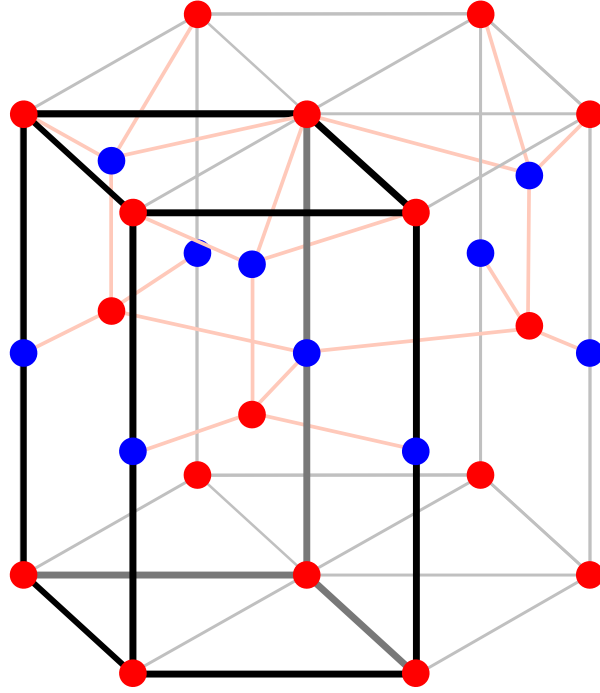
Normally group III-V semiconductors tend to crystallize into zinc blende (ZB) crystal structure shown in figure 2.2. It is common for a number of compound semiconductors such as GaAs, AlAs, InP, GaP. ZB consists of two face-centered cubic lattices where red spheres represent group V atoms (e.g. As) and blue spheres define group III atoms (e.g. Ga). ZB is very similar to diamond crystal structure except for the fact that in diamond structure

atoms of the basis are identical. For example, diamond crystal structure is common for elemental semiconductors such as silicon, germanium and carbon. [4, p. 7-8]



**Figure 2.2:** Schematic illustration of zinc blende (ZB) crystal structure which is typical for group III-V semiconductors. Red spheres represent group V atoms and blue spheres define group III atoms. ZB is formed by interpenetration of two face-centered cubic lattices.

Wurtzite (WZ) crystal structure, illustrated in figure 2.3, is an example of hexagonal unit cell. It is encountered in a number of compound semiconductors such as ZnO, AlN, GaN. Since ZB and WZ are energetically close to each other, III-V semiconductor NWs can exhibit either ZB or WZ or the mix of both crystal structures depending on growth conditions such as seed particle size, V/III-ratio, precursor flow, temperature and doping [5–8].



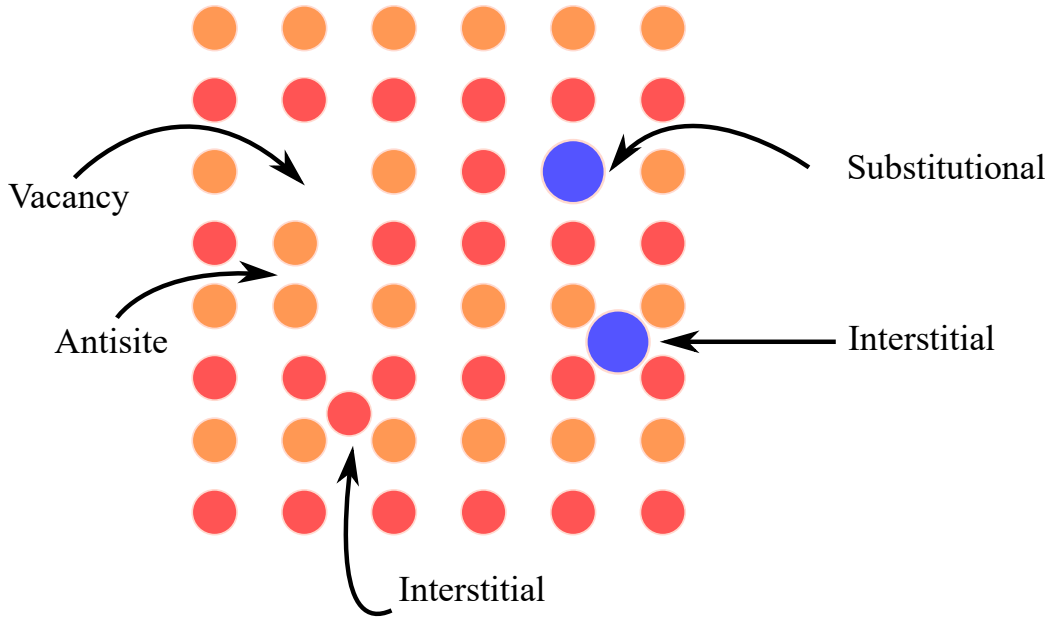
**Figure 2.3:** Schematic illustration of wurtzite (WZ) crystal structure which is a hexagonal unit cell. Red spheres represent group V atoms and blue spheres define group III atoms.

## 2.2 Defects in semiconductors

It has to be said that in reality ideal crystals do not exist and there are always imperfections or defects. While some defects can be useful (semiconductor doping impurities), others may significantly degrade device performance and hence must be considered and controlled. Generally, defects can be classified into several categories: point defects, line defects, planar defects and volume defects.

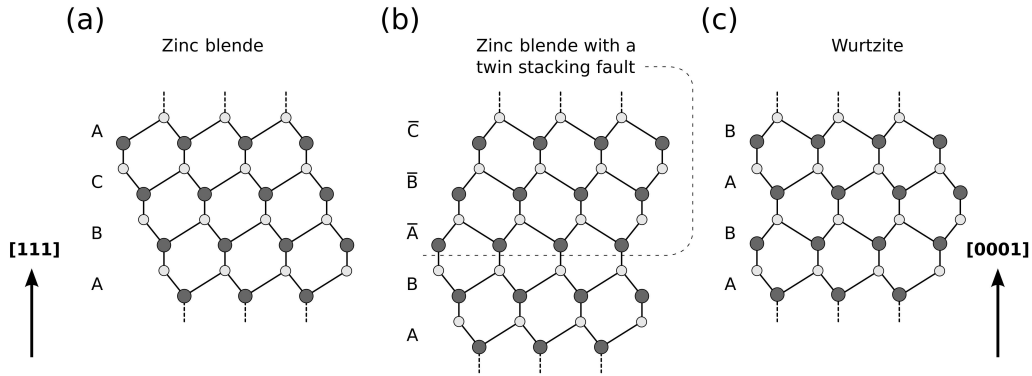
Point defects (presented in figure 2.4) are highly localized and only involve isolated atoms. They can be further divided into subcategories such as vacancies, antisites, interstitial and substitutional defects. Vacancy forms when an atom is missing from a lattice point while antisite is created when different types of atoms exchange the positions. Vacancies and antisites are considered to be native defects since foreign atoms are not involved. Interstitial defect is formed when native or impurity atom occupies empty space

between the lattice atoms while substitutional defect is created when impurity atom replaces the host atom at its regular place in the crystal structure. Hence, interstitial and substitutional defects are called extrinsic defects. [9, p. 159-161]



**Figure 2.4:** Schematic drawing of main point defects in crystals including vacancies, antisites, interstitial and substitutional atoms. As an example, orange spheres represent Ga atoms, red spheres stand for As atoms and blue spheres depict impurity atoms.

On the contrary to point defects, line defects (also referred as dislocations) involve rows of atoms connected by line. Dislocations are generated when lines of atoms are misaligned or displaced with respect to the crystal lattice which happens due to stress. Planar defects are associated with imperfections that exist in a large volume of the crystal. Typical planar defects include stacking faults and twin planes, antiphase and grain boundaries, interfaces. Volume defects are connected with bulk crystal growth quality which could result in formation of amorphous or void regions. [4, p. 16-18]



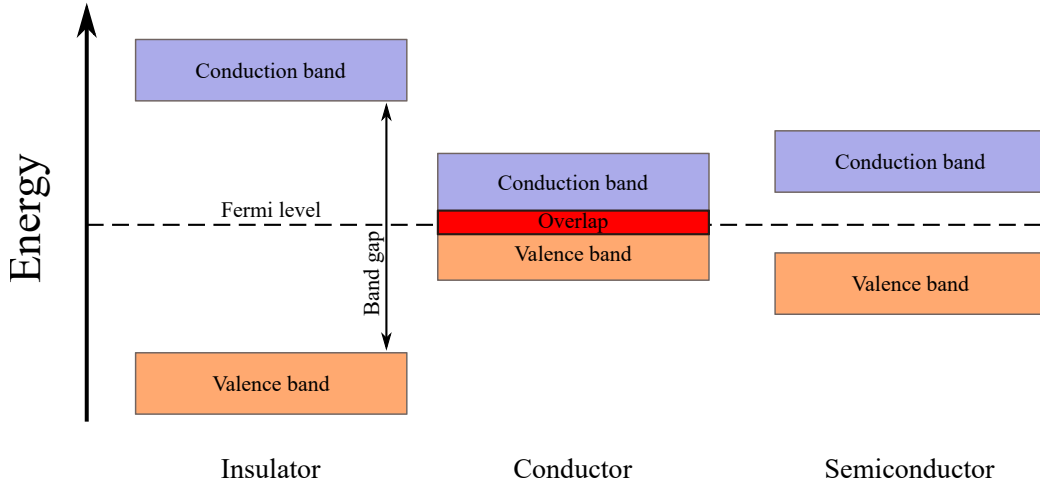
**Figure 2.5:** Schematic drawing of the planar projection of (a) zinc blende crystal structure, (b) zinc blende crystal structure with twin stacking fault and (c) wurtzite crystal structure. Copied from [10].

The alternating ZB and WZ phases in NW crystal cause stacking faults and twin planes which are the most common defects in nanowires. As shown in figure 2.5, ZB structure is a sequence of layers ABCABCABC... along the  $[111]$  direction. Once the twin stacking fault is introduced, it rotates the crystal by  $180^\circ$  around the growth direction and results in  $AB\bar{A}\bar{B}\bar{C}$  sequence for ZB. In fact, high number of consecutive twin plane formations in ZB crystal can result in WZ structure whose layers follow ABABAB... sequence. [11] Although, the growth parameters can be tuned to realize a single-phase crystal structure in NWs, often this is an extremely challenging task. Stacking faults and twin planes create non-radiative recombination centers which affect optoelectronic performance of NWs. As a result, crystal structure quality can have a strong effect on optical and electrical properties of NWs. For example, there are reports that crystal phase mixing can dramatically increase NW resistivity [12], lower carrier mobility [13] and strongly diminish photoluminescence intensity and open circuit photovoltage [14].

## 2.3 Electronic band structure: optical and electrical properties of semiconductors

Electronic band structure is a concept that is used to describe the behaviour of electrons in solids. Once isolated atoms with discrete energy levels are brought together into a crystal structure, their atomic orbitals start to overlap, thus forming separated energy levels for each level of the isolated

atom. This happens due to Pauli exclusion principle which asserts that no two electrons in a solid can have same energy states. Consequently, the energy levels are split into allowed continuous bands that are separated with forbidden band gaps - energy ranges where electron states cannot exist. Although there can be numerous allowed bands in a solid, the two most significant energy bands are valence band and conduction band (presented in figure 2.6). Valence band is the highest occupied energy band that is generally filled with electrons at absolute zero temperature. Conduction band is the lowest unoccupied band that is generally empty at absolute zero temperature (0 K). Therefore, the forbidden band gap is defined as the difference between the highest point of the valence band and the lowest point of the conduction band. [15, p. 163, 187]



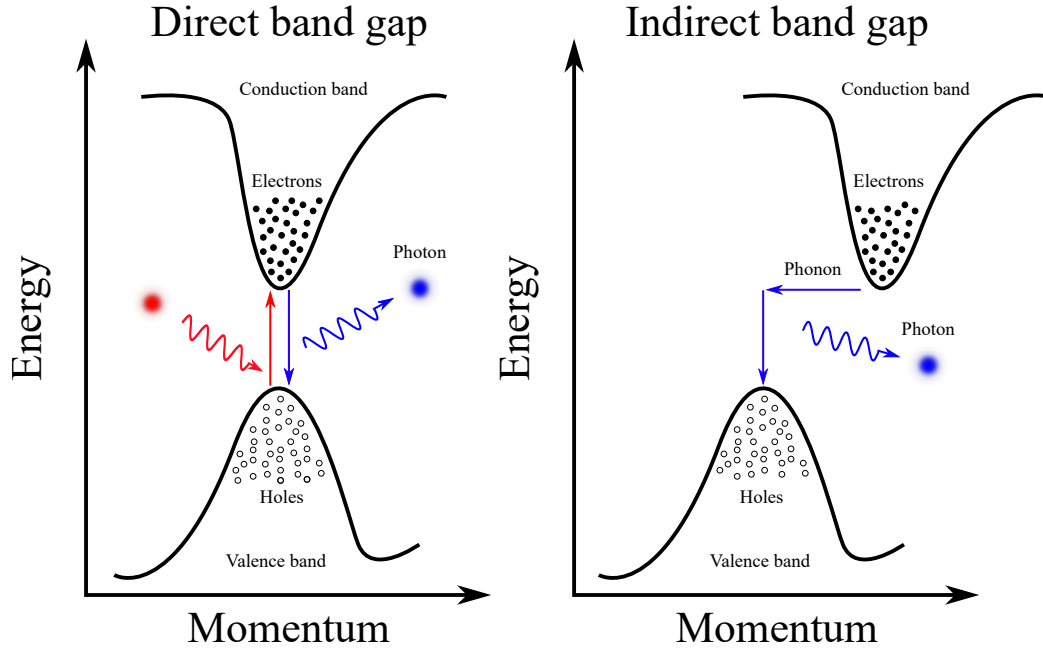
**Figure 2.6:** Schematic illustration of electronic band structure concept in solids. Valence band is defined as the highest band fully occupied with electrons at 0 K. Conduction band is the lowest unoccupied band at 0 K. Band gap represents the energy difference between the conduction band and the valence band. Depending on the Fermi level and the number of charge carriers at allowed energy bands, solids are categorized into conductors, semiconductors and insulators.

Electrical conduction arises from the motion of charge carriers within allowed energy bands. The electrical properties of the material are defined by electronic band structure as they directly depend on the population of electrons at each energy band. Based on this, solid materials can be classified into three categories: conductors, semiconductors and insulators (depicted in figure 2.6). Semiconductors have some number of electrons both at valence

band and conduction band which can be varied with doping. On the contrary, insulators have either filled or empty allowed energy bands which cannot contribute to electrical conductivity as there are no free carriers and hence no current flow. That is also why semiconductors are effectively insulators at 0 K. However, as the temperature increases, electrons in semiconductors are thermally excited and promoted from valence band to conduction band crossing the narrow energy band gap. In case of insulators, the thermal energy is not enough as the band gap is substantially larger. In conductors filled band overlaps with an empty band resulting in two partly filled bands and, thus, good electrical conduction even at 0 K. [4, p. 61]

The location of the Fermi level can be used to determine electrical properties of the material. Fermi level is a conceptual electron energy level which has 50% probability of being occupied at any given time at thermodynamic equilibrium. Fermi level is constant across the whole crystal. In conductors Fermi level is located within the overlap region full of current carrying states while in insulators it is located within the band gap away from any energy states (displayed in figure 2.6). In undoped semiconductors, Fermi level is located exactly in the middle of the band gap, close enough to both bands to be thermally populated with electrons or holes. Moreover, by doping the semiconductor, one can shift the energy bands relative to the Fermi level resulting in increased free carrier concentrations. [4, p. 95-99]

Electronic band structure is also used to determine the optical properties of the material. In band diagrams the energy is plotted as a function of electron momentum (according to Bloch's theorem). The band gap of semiconductor can be either direct or indirect (schematically illustrated in figure 2.7). In direct band gap semiconductors, the valence band maximum and the conduction band minimum occur at the same value of electron momentum. In indirect band gap semiconductors, the valence band maximum occurs at a different value of electron momentum than the conduction band minimum. The concept of direct and indirect band gap plays a big role in the processes of carrier recombination and generation. [15, p. 188-189]



**Figure 2.7:** Schematic drawing of direct and indirect band gap concept as well as carrier generation and recombination processes. When light is absorbed, it excites the electrons from valence band to conduction band. This is called carrier generation. In an inverse process of recombination, the electrons experience transition from conduction band to valence band, radiating the photons that have energy equal to the band gap. However, this is mainly the case in direct band semiconductors since electron momentum change is not required. The probability of radiative recombination in indirect band semiconductors is low. For this reason, optoelectronic devices are fabricated from direct band semiconductors.

Carrier generation and recombination are fundamental processes that occur during light absorption and emission in optoelectronic devices. Carrier generation take place when the absorbed photon with the energy equal or higher than the band gap excites an electron from the valence band to conduction band (as shown in figure 2.7). As a result of this transition, electron-hole pair is created. Hole is a positively charged vacancy left by the electron which is actually a quasiparticle that is used to simplify the concept of semiconductor operation. Both electrons and holes contribute to electrical conduction in semiconductors.

Recombination is a reverse process that occurs when electron jumps back to the valence band, and as a result of this transition, electron-hole pair is annihilated and photon with energy corresponding to the band gap is

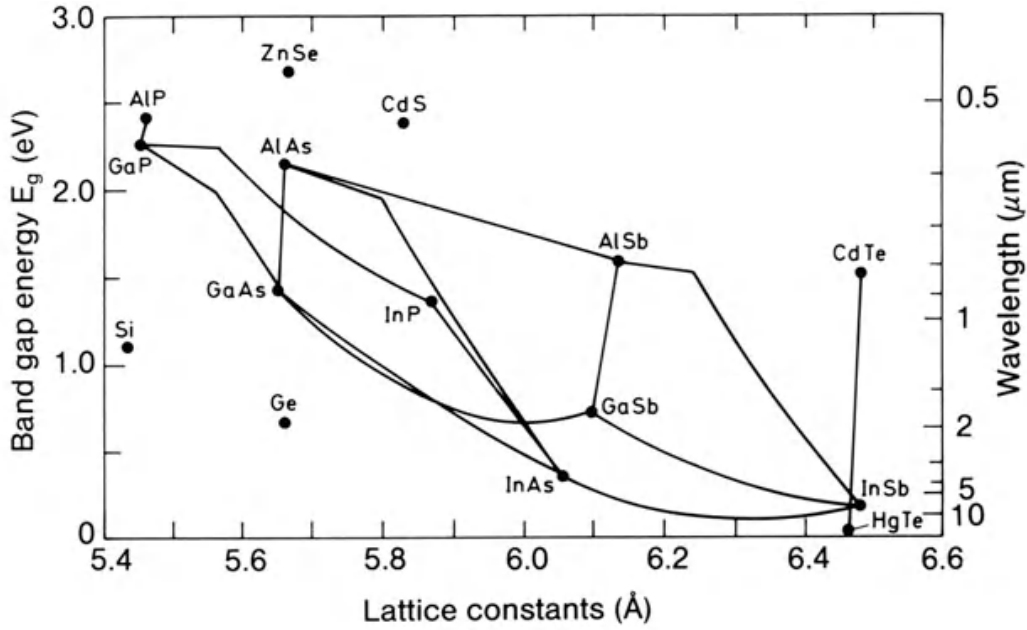


released. There are several types of recombination which can be divided into radiative and non-radiative. In radiative recombination, the energy is released in form of a photon as mentioned above. However, in the case of non-radiative recombination, the resulting energy can be either transferred to another charge carrier (Auger recombination) or it can be trapped in the intermediate energy level within the band gap caused by defect (Shockley-Read-Hall recombination). [4, p. 211-214]

A striking point is that in direct band semiconductors the transition of electron does not require a change in momentum, and for this reason, the probability of radiative recombination and generation is much higher. Hence most optoelectronic devices are based on direct band semiconductors which enable efficient light absorption and emission. Radiative recombination is also possible in indirect band semiconductors, but for that the electron must change its momentum by interacting with phonon (lattice vibration) and the probability of photon emission is much lower.

## 2.4 III-V compound semiconductors

Compound semiconductors are semiconductors that consist of several different elements. Binary (GaAs, InP, GaN), ternary (InGaAs, AlGaAs) and quaternary (InAlGaAs, AlInGaP) semiconductors are composed of two, three and four elements respectively. Figure 2.8 illustrates parameters of several most important elementary and binary semiconductors commonly used in optoelectronic devices. Band gap energy at room temperature (RT) and corresponding wavelength are plotted against lattice constant. The lines represent the band gaps of ternary compounds that can be obtained from corresponding binary semiconductors with different ratios. In fact, by forming compound alloys, it is possible to effectively tune the band gap energy according to required absorption and emission ranges. [4, p. 78-80]



**Figure 2.8:** Schematic drawing of several most important elementary and binary semiconductors commonly used in optoelectronic devices. Energy band gaps and corresponding wavelengths are plotted against lattices constants. Connecting lines represent the band gaps of ternary compounds that can be formed from corresponding binary semiconductors with different ratios. Reprinted from [16].

III-V compound semiconductors are formed by combination of group III (Al, Ga, In) and group V (N, P, As, Sb) atoms in the chemical table. Table 2.1 shows the band gaps, crystal structures, and carrier mobilities of some elementary and III-V compound semiconductor materials at RT. Mobility is the magnitude of the charge carrier velocity per unit electric field. In other words, mobility defines how fast can carriers move through a material with the application of an electric field which directly affects the performance of the device. Actually, both electron and hole mobility contribute to the total electrical conductivity of the material. [15, p. 208]

**Table 2.1:** Band gaps, crystal structures, and carrier mobilities of some elementary and III-V compound semiconductor materials at RT. Lattice constants  $a$  and  $c$  represent different directions of the WZ crystal. Data was acquired from [17].

Material	Band gap (eV)	Lattice constant (Å)	Electron mobility (cm <sup>2</sup> /(V s))	Hole mobility (cm <sup>2</sup> /(V s))	Crystal structure	Band gap type
Si	1.12	5.431	1400	450	Diamond	Indirect
C	5.5	3.567	2200	1800	Diamond	Indirect
Ge	0.66	5.658	3900	1900	Diamond	Indirect
GaAs	1.42	5.653	8500	400	ZB	Direct
GaSb	0.72	6.095	3000	1000	ZB	Direct
GaP	2.26	5.450	250	150	ZB	Indirect
InP	1.34	5.868	5400	200	ZB	Direct
InSb	0.17	6.47	77000	850	ZB	Direct
AlN	6.2	$a=3.111$ $c=4.981$	300	14	WZ	Direct
GaN	3.2	$a=3.160$ $c=5.125$	1000	350	WZ	Direct

Looking at the table, we can see that III-V compound semiconductors have a band gap roughly between 0.5 eV and 6 eV which makes them particularly useful in absorption and emission of energies between near infrared and near ultraviolet ranges. Moreover, very high carrier mobilities, direct band gap and the ability to precisely engineer the band structure by alloying two or more elements make III-V compound semiconductors particularly invaluable and dominating in fabrication of high performance optoelectronic devices. For this reason, mainly group III-V semiconductors are used for nanowire synthesis in pursuit of novel applications. The advantage of heteroepitaxial growth of III-V semiconductor NWs is that, due to lateral strain relaxation, they can be defect-free when different crystalline materials with very different lattice constants are used [18]. As a result, complex nanostructures such as modulation-doped NW superlattices can be fabricated on different growth substrates [19].

## 2.5 Intrinsic and extrinsic semiconductors

As was stated in section 2.3, semiconductors are effectively insulators at 0 K because their valence band is completely filled and conduction band is totally empty. Consequently, there are no free carriers that can conduct current. As the temperature rises, electrons are thermally excited to conduction

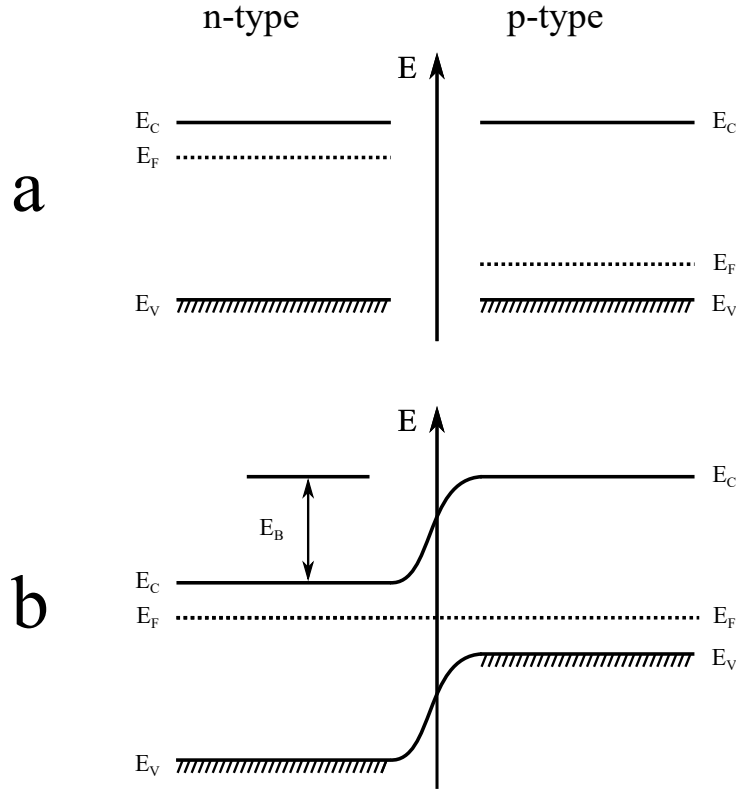
band which results in equal partial filling of both bands at RT. Such carriers are called intrinsic and a semiconductor is considered intrinsic when it does not contain significant amount of impurities. However, intrinsic carrier concentrations are too low for current densities that are required for practical devices. Furthermore, electrical conductivity of intrinsic semiconductors is very dependent on the temperature and it cannot be effectively controlled by external electric fields. Hence, in order to increase free carrier densities, dopant atoms are required. [4, p. 95-99]

Extrinsic (or doped) semiconductors are semiconductors that contain a significant number of foreign atoms incorporated by doping. Doping is a fundamental process of deliberate introduction of impurities into the crystal structure of the semiconductor which dramatically changes its electrical properties. Dopant impurities can be either donors or acceptors. Donor atoms have extra electrons while acceptors have fewer electrons (or extra holes) than the atoms they replace. As a result of doping, n-type regions with higher electron carrier concentration and p-type regions with higher hole carrier concentration can be obtained. Apparently, this leads to high concentration of carriers and high electrical conductivity. For example, intrinsic silicon can become n-type if it is doped with phosphorous (donor) which has one extra valence electron, or it can become p-type if it is doped with boron (acceptor) which has one extra hole. [15, p. 209-2011]

## 2.6 The p-n junction

Extrinsic semiconductors are essential for fabrication of modern electrical and optoelectronic devices. In particular, p-type and n-type regions of the same semiconductor material are used to create p-n junctions which are primary building blocks of most solid-state devices such as transistors, light-emitting diodes (LED), diodes, lasers, solar cells and many more. Figure 2.9 (a) shows an imaginary case of n-type and p-type regions before they are combined together where  $E_C$  and  $E_V$  represent conduction and valence band energy levels while  $E_F$  defines the Fermi level. Once the n-type and p-type regions are joined together, they form a junction which causes energy bands to bend in order to maintain the same Fermi level across the junction at thermodynamic equilibrium (shown in figure 2.9 (b)). Additionally, a depletion region is formed near the p-n interface because of the diffusion of holes into the n-type region and the diffusion of electrons into the p-type region. Depletion region does not have any free charge carriers as it only consists of negatively and positively charged ions that are created due to diffusion. These ions create an electric field that opposes further diffusion and results in formation

of potential difference ( $E_B$ ) across the junction at equilibrium condition. [16, p. 297-299]



**Figure 2.9:** Schematic drawing of the p-n junction. (a) Imaginary case of n-type and p-type regions before the merge.  $E_F$  is the Fermi level,  $E_C$  and  $E_V$  represent conduction and valence bands. (b) The p-n junction after both regions were merged together. Band bending occurs in order to maintain the same Fermi level across the junction and built-in potential  $E_B$  is formed after equilibrium is reached.

The situation changes when the external potential is applied across the junction. The p-n junction is forward biased when the p-type region is connected to the positive voltage in comparison to the n-type region and the junction is reverse-biased otherwise. Reverse bias increases band bending and causes depletion region to wider even further, enlarging the junction electrical resistance and effectively making it an insulator. On the contrary, forward bias reduces band bending and causes depletion region to shrink, minimizing the electrical resistance and allowing the charge carrier (current)

flow across the junction. Thus, basically a traditional p-n junction acts as a rectifying diode that conducts current only in one direction.

## Chapter 3

# Semiconductor nanowires

This chapter presents the theory behind III-V semiconductor nanowires. Section 3.1 describes epitaxial growth of NWs governed by vapour-liquid-solid method and effects of growth conditions are discussed in section 3.2. Surface states and passivation of NWs are presented in section 3.3 and NW doping is described in section 3.4. Finally, sections 3.5-3.7 discuss NWs based applications and, in particular, next generation solar cells.

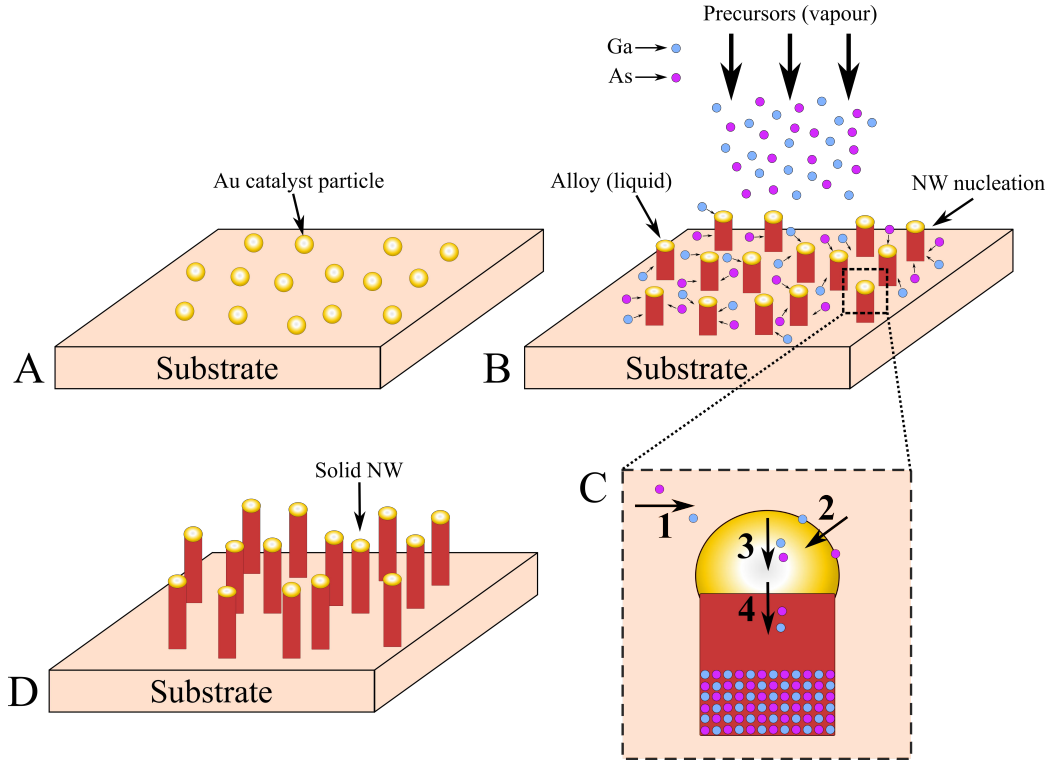
### 3.1 Vapour-liquid-solid growth mechanism

There are two approaches to fabricate NWs: so called “top-down” and “bottom-up” methods. Traditional top-down microfabrication approach employs lithography to etch nanostructures from bulk materials. Although the method is superior in NWs definition and placement [20], it has severe limitations on feature size and NW growth control. Also, the top-down etched nano pillars suffer from a very rough surface thereby opening non-radiative recombination channels. On the contrary, bottom up approach is most widely used as it relies on self-assembly process that mimics nature and enables precise control and tuning of NW material, morphology, crystal structure, doping and other crucial parameters. [21] In self-assembly, nanowires down to 5 nm in diameter can be synthesized.

Vapour-liquid-solid (VLS) mechanism is one of the most developed and widely used single crystal growth bottom up methods that has been suggested already in 1964 and have dominated in creation of nanowires, whiskers, rods and other one-dimensional structures [22]. A variety of different techniques can be used to facilitate VLS NW growth. The most prominent include metalorganic vapour phase epitaxy (MOVPE), chemical beam epitaxy (CBE), molecular beam epitaxy (MBE) and chemical vapour deposition (CVD). As

can be seen from its name, VLS growth involves three phases: vapour-phase precursor, catalytic liquid alloy and solid crystal. The principal schematic of the VLS mechanism is presented in figure 3.1. In this method, metal seed particles (typically Au), that are deposited onto the substrate, form alloy droplets with the substrate material at elevated temperatures. For reasons, which are yet not fully understood, these droplets become supersaturated with continuously supplied vapour-phase precursor molecules and eventually act as nucleation sites for one dimensional crystal growth. The kinetic processes in VLS growth include: (1) mass transport from the vapour phase (2) precursor molecule decomposition at vapour-liquid interface (3) atom diffusion in the liquid phase and (4) atom incorporation in a crystal. [23]





**Figure 3.1:** Schematic illustration of the vapour-liquid-solid (VLS) mechanism and III-V compound semiconductor NWs growth as an example. (a) Metal catalytic particles (Au) are deposited onto the substrate. (b) At elevated temperatures, they form alloy droplets with the substrate material. As vapour-phase precursor molecules (Ga and As) are continuously supplied, Au droplets become supersaturated and eventually act as nucleation sites for NW crystal growth (c). (d) The kinetic processes in VLS can be described in four steps: (1) mass transport of precursor molecules from the vapour phase to the catalyst particle (2) precursor decomposition at vapour-droplet interface (3) atom diffusion in the Au droplet and (4) precursor atom incorporation in a crystal.

### 3.2 Effect of growth conditions

VLS NW growth depends on a number of growth parameters such as temperature, V/III precursor ratio, growth time, total molar flow, pressure and catalyst nanoparticle size and density. The variation of these parameters may lead to NWs with significantly different morphologies and crystal structures as well as electrical and optical properties. Essentially, the trade-off between

such parameters and tailoring of numerous growth conditions are needed in order to achieve optimal NWs depending on applications requirements.

Growth temperature is perhaps the most crucial parameter that affects NW synthesis. It has to be said that VLS NW growth occurs within specific temperature range, usually between 300 °C and 500 °C. The lower limit is dictated by the temperature of the precursor decomposition while the upper limit defines the transition from axial to radial or thin film growth. NW is considered tapered (cone shaped) when the base diameter is bigger than the tip diameter. Tapering is undesirable for many device applications that require a uniform diameter such as lasers and single nanowire solar cells. At higher temperatures NWs tend to experience severe tapering that increases exponentially [24–26]. Tapering can be minimized by using low growth temperature and optimized growth parameters. What is more, a lower growth temperature substantially decreases the density of twin defect. Also, it is widely reported that low growth temperature results in minimum radial growth, improved optical properties and crystal quality [8]. However, it is a trade-off as at the lower growth temperatures NWs are kinked and irregular. [24, 27] The increase in temperature leads to increase in growth rate and NW length and may even lead to transition of crystal structure from ZB to WZ [28–30]. Interestingly, the combinations of both low and high temperatures steps in a growth process may lead to superior quality NWs [8, 31].

Another important parameter that drastically affects NW growth is V/III precursor ratio. High V/III precursor ratios usually result in decrease of NW twin density or no crystallographic defects at all and thus better optical properties. However, if V/III ratio is too high, NWs become kinked and tapered. Moreover, NW growth direction depends on V/III ratio: low ratio leads to vertical [111] which is often desired. On the contrary, high V/III ratio promotes non-vertical orientation during NW growth. Furthermore, the carbon impurities that are inherited in MOVPE growth are reported to decrease as V/III ratio increases. [32] V/III precursor ratio also affects the crystal structure as NWs with high V/III precursor ratio tend to exhibit ZB while low V/III precursor ratio supports WZ growth [5]. In addition, there are reports that growth rate increases as V/III ratio increases but then drops after certain maximum is reached [28, 33].

Other factors that affect the growth include total flow rates, pressure and catalyst particles size and density. High precursor flow rates result in high growth rate and lead to decreased tapering and high yield of vertical NWs [7, 34]. High (or rapid) growth rate is reported to significantly improve NW morphology and crystal structure as well as optical properties [7]. Additionally, the growth rate depends on catalyst NP size and distribution as well

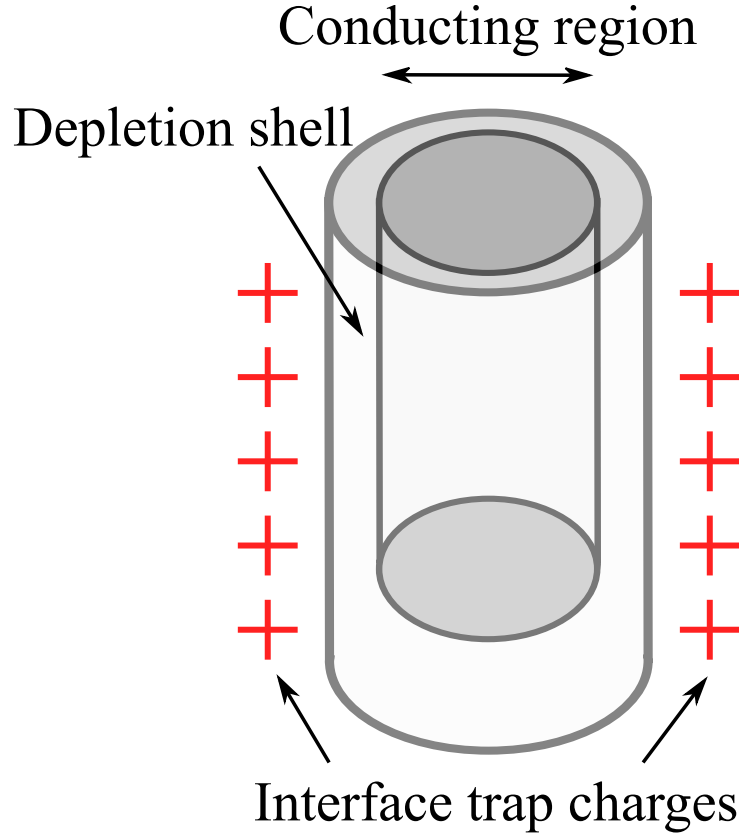
as NW density [25, 33]. Although the studies are scarce, it is also reported that NW growth can be seriously affected by reactor pressure. Generally, higher pressure leads to higher growth rate [35]. Higher pressure may also lead to improved crystal quality but higher degree of tapering [36]. However, the optimal and stable results are usually achieved at low or near atmospheric pressure which is predominantly used in VLS NW growth.

The use of Au as catalyst particle has been prevailing since the earliest work concentrated on this material and it is well-developed catalyst for many NW materials. Furthermore, Au is typically better than other metals in producing well-oriented, size-selected nanowires. Au is also inert and does not react with oxygen or gas-phase carriers. [37] Though there are conflicting reports, according to some, the disadvantage of Au as a catalyst metal is that it is undesirable contaminant in semiconductor processing and can be detrimental in optoelectronic applications because it can increase the impurity level in the band gap. For these reasons, catalyst free growth can be also considered. Catalyst free growth could be done using A droplets from  $A_xB_y$  compound. For instance, in situ deposited indium droplets are used for InP nanowires growth. Nevertheless, catalyst-free method has demanding restrictions on the growth conditions and material compositions outside binary compounds [10, 23]. Moreover, when Au is used as catalyst for NW growth, it can be removed from the top end of the NWs by etching [38].

### 3.3 Surface states and passivation

Surfaces play a crucial role in semiconductor properties. As there are almost no ideal surfaces in real life, typically, surface bonds try to readjust towards a configuration with a minimum energy. As a result, there is a bond disorder and some of the bonds are left unoccupied or “dangling”. [4, p. 13-16] The role of the surfaces is even more profound in NWs that have extremely high surface-to-volume ratio. A major problem associated with NWs is the formation of high density of surface states which appears due to unpassivated dangling bonds. Basically, the surface states act as non-radiative recombination centers and make additional electronic states (surface charged traps) within the band gap that cause bending of the Fermi level at the surface of the NW and push the free carriers from surface to the bulk [34]. Thus, undesirable depletion layer is formed which limits the movement of free carriers and has detrimental effects on device operation (depicted in figure 3.2). What happens is that the surface states can cause the depletion layer to extend to the whole NW diameter, effectively making it semi-insulating and unusable for device applications or drastically changing its electrical, optical and

mechanical characteristics [34, 39, 40]. The effect is especially pronounced in III-V NWs including GaAs which is the most widely used in optoelectronics and photovoltaics [41–43]. Actually, GaAs has surface recombination velocity (SRV) of  $10^5$  cm/s which is dramatically higher than SRV of InP (170 cm/s) [44, 45]. Hence, it is particularly critical to address surface states limitation in GaAs NWs applications.



**Figure 3.2:** Schematic illustration of surface depletion layer in a single nanowire resulting from Fermi level pinning due to surface states. The surface states can cause the depletion layer to extend to the whole NW diameter, effectively making it semi-insulating and unusable for device applications.

However, the problem can be eliminated by means of surface passivation methods [46]. One prevailing way that can provide long-term surface stability is passivation of GaAs NWs with wide band gap lattice matched semiconductors such as AlGaAs [43, 47], InGaP [48–50], AlInP [51, 52]. As a result, nanowires exhibit a significantly longer lifetime due to the passivation of surface states as well as dramatic enhancement in the PL intensity

and increase in the minority carrier diffusion length [43, 47]. Passivation is especially important for NWs in solar cells applications as it reportedly provides substantial performance and efficiency improvements [50, 53]. Another potential passivation method is in situ growth of non-lattice machined InP or GaP capping layers. It is reported that even a few monolayers of such layer provide an efficient passivation with small effect on the morphology and band structure [42]. However, the long-term stability suffers a lot, hence, the method is applicable only as a short-term solution [41].

Passivation can be performed either in situ or ex situ. In situ passivation is done inside the MOVPE reactor as a thin film shell is wrapped around the NW at elevated temperatures, typically exceeding 600 °C. In situ passivation is usually preferred since it allows epitaxial and control growth of passivation layers. Ex situ passivation is performed outside the growth reactor and atomic layer deposition (ALD) is commonly used. Ex situ passivation in ALD allows the use of wider range of materials which are not available in MOVPE such as dielectrics and biocompatible coatings.

### 3.4 Doping of nanowires

Doping is an essential step in fabrication of NW based devices. Naturally, doping of NWs is done in situ during the actual synthesis. In MOVPE, dopant precursors are supplied into the reactor together with the main growth elements where they decompose and substitute some of the atoms in the semiconductor. Depending on the dopant, the resulting material can be either n-type or p-type. For example, group II elements such as Zn (supplied as DEZn precursor) are widely used for p-type NW doping while group IV elements such as Si or Sn (supplied as Si<sub>2</sub>H<sub>6</sub> and TESn precursors) are used for n-type NW doping. The dopants may be incorporated into the material either due to transport via the metal seed particle, or at the particle/nanowire interface, or via diffusion through the side facets. [31]

It has to be said that the doping of NWs is considerably more complicated than doping of the bulk materials because of the Au catalyst droplet and it requires a detailed understanding and control. First, high surface-to-volume ratio of the NW, Au droplet acting as catalyst and the surface states associated with it can affect the doping process. As dopants incorporate into the nanowires via the Au droplet, the solubility of group III and group V source adatoms makes the doping process challenging. The group III adatoms are directly soluble with Au, therefore they incorporate directly, while the group V adatoms are not soluble, so they incorporate via the sideways of the Au droplet. Also, dopants have a tendency to segregate at the surface of the un-

passivated NWs leading to significant decrease of the carrier concentrations and hence conductivity. Consequently, larger dopant concentrations may be required. [54] Also the location of dopant incorporations in NWs is reported to be strongly diameter dependent and inhomogeneously distributed along the radial direction [55]. Furthermore, doping has a dramatic effect on NW synthesis. There are numerous reports on effects of DEZn doping of nanowire growth rate, growth direction, crystal structure, defect density and morphology, electrical and optical properties [31, 56–59].

Controlled and uniform doping is notably crucial for radial p-n junction NW solar cells upon which their performance is deeply dependent. High doping levels may be required to avoid forming of the depletion layer. Although power conversion efficiency (PCE) does not change with increasing doping concentration, it can drop substantially if certain doping level is not reached [60]. Additionally, sufficiently high core doping is needed for carrier collection at core-shell junction otherwise carrier collection at core-substrate junction is dominant and, hence, the advantages of core-shell radial junction are not exploited. High doping may lead to lower carrier lifetime, however it is reported that doping level has a dramatically higher effect on PCE than the carrier lifetime. [61]

### 3.5 Current progress in nanowire devices and applications

The unique properties of NWs open up completely new perspectives for the variety of novel devices for different applications. Although NWs have not reached the industrial scale production yet, a number of conceptual devices based on single nanowire or an array of NWs have been demonstrated over the past years.

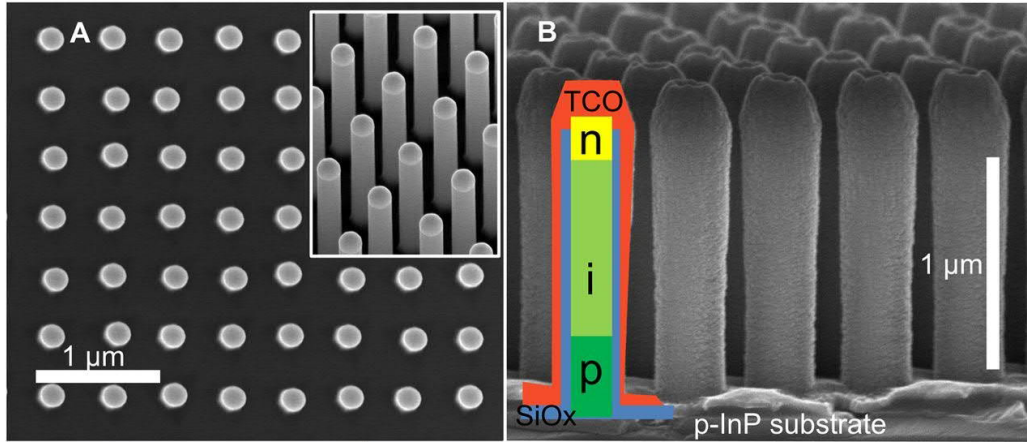
A lot of work have been focused on development of NW based field-effect transistors (FET). FETs are fundamental building blocks of electronics which quantity on an integrated circuit is predicted to double every two years according to Moore's law [62]. However, due to limitations of conventional lithographic fabrication methods, it is difficult to keep the trend as transistor scaling reaches its physical limits. NW based FETs is an alternative solution that can offer perfectly controlled high efficiency nanoscale devices being compatible to current Si-based electronic processing techniques. The first successful NW FETs have been demonstrated already at the start of the millennium [63, 64], followed by development of highly scalable wrap-gate NW FETs with lateral and vertical channel geometries [65–68].

Moreover, there has been a tremendous progress in NWs research in the field of photonics and its diverse applications. NWs have been identified as a next frontier in optoelectronics and as a novel alternative to conventional waveguides, optical cavities, filters and other primary building blocks of photonics offering better performance, low cost and low power consumption. In particular, NWs act as excellent resonant cavities providing low-gain threshold values and high quality factors [69]. Thus, NW based lasers were successfully demonstrated over the past years [70–73]. Furthermore, direct band growth materials and ability to tune the band gap across ultraviolet, visible and infrared spectral regions enabled the realization of NW based LEDs that have large light-extraction efficiency and low defect density [74–77].

Additionally, studies from a number of research groups demonstrated a range of intriguing applications outside optoelectronics such as biological [78–80], chemical [81–83], molecular sensors [84–86]. What is more, NWs have been used as electromechanical resonators [87], piezoelectric and thermoelectric nanogenerators [88, 89] as well as in lithium-ion batteries applications [90, 91]. However, probably the most groundbreaking application of NWs is the next generation of photovoltaic cells.

### 3.6 Solar cells based on semiconductor nanowires

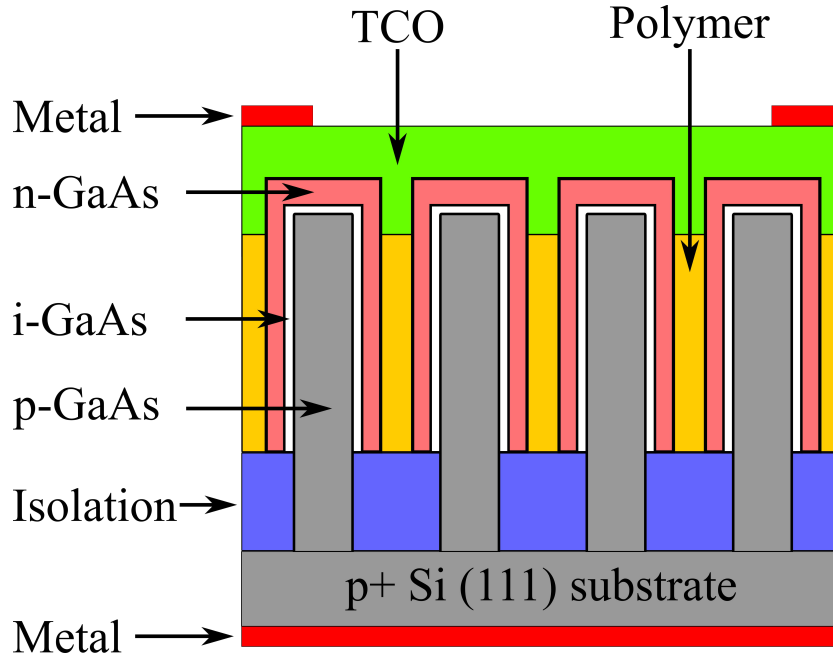
III-V semiconductor nanowires are being extensively researched as excellent candidates for fabrication of the next generation solar cells [53, 60, 92–94]. Not only can they dramatically improve the efficiency of the novel devices, but also they can lower the cost of the conventional Si based solar cells used nowadays. Due to the unique properties (direct band gap, high carrier mobility) and dimensions on the scale of visible light wavelengths, nanowires allow superior light absorption and charge collection as they practically act as light concentrators. Single nanowire can concentrate 15 times the sun light according to some reports [95]. Additionally, the use of NWs eliminates the need for anti-reflective coatings. [96, 97]



**Figure 3.3:** State of the art nanowire array solar cell with 13.8% efficiency reported by Wallentin et al. Copied from [92].

Integration of NWs on lattice mismatched Si substrates and even cheap glass substrates allows to dramatically cut materials costs and achieve superior efficiencies by using both sides of the solar cell with the help of transparent conductive oxides (TCO) [60]. Thus, nanowires can even exceed the maximum theoretical efficiency limit (Shockley-Queisser) of 34% for a single p-n junction solar cell [95, 98]. At the moment, the best NW based solar cell show photovoltaic conversion efficiency of 17.8%, which will certainly rise in the near future [99]. For example, figure 3.3 shows state of the art InP nanowire array solar cell with 13.8% efficiency reported by Wallentin et al. [92].





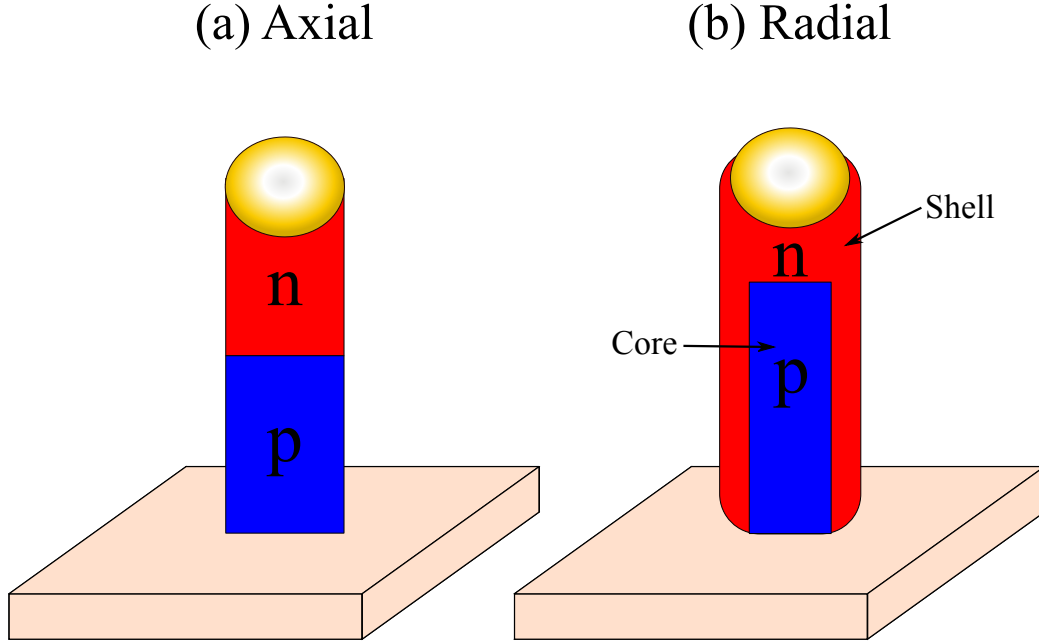
**Figure 3.4:** Schematic illustration of the planarization scheme for III-V NW solar cell fabrication on Si substrate.

Both figure 3.3 and figure 3.4 are good examples of planarization schemes for III-V NW solar cells fabrication. First, ordered NW arrays are epitaxially grown on either lattice matched or lattice mismatched substrates. Nanoimprint lithography or electron beam lithography can be used to arrange the catalyst seed particles in arrays. It is crucial to apply an isolation layer to allow contact separation between p- and n-type regions. Nominally intrinsic region can be grown to increase the absorber area and reduce the interfacial recombination. Additionally, a polymer layer can be spin coated to fill the void between the NWs, and the metal seed particles can be removed to reduce the reflection. Finally, TCO is used as a top contact. Interestingly, the figures also represent two fundamentally different fabrication approaches that are mostly used for NW based solar cells.

### 3.7 Axial and radial p-n junctions

There are two NW geometries that can be used for the next generation solar cell applications: axial and radial p-n junction NWs (shown in figure 3.5). As the p-n junction is a fundamental part of the solar cell, it must be introduced within the NW, in order to promote charge separation and collection. In axial

NWs, the junction occurs along the length of the nanowire, while in radial NWs (core-shell), the junction is formed along the diameter i.e. core is n-type doped while the shell is p-type doped or vice-versa. [100]



**Figure 3.5:** Schematic illustration of the NW p-n junction geometries that are mainly used for solar cell applications (a) Axial NW structure with opposite doping along the axis. (b) Radial nanowire structure with opposite doping of shell and core. Blue and orange colours denote different types of doping.

Comparing these two configurations, the main advantage of using radial p-n junction NWs in solar cell applications is the radial charge separation, increased defect tolerance, and most importantly, far larger active area than the axial p-n junction. In particular, the light absorption occurs along the whole NW length (few microns). Moreover, carrier collection distance is smaller or comparable to the minority carrier diffusion length in radial p-n junction. Hence, photo generated carriers only need to travel the radial distance and can be separated and collected with high efficiency without substantial bulk recombination. [96] Despite the advantages, radial NWs bring some challenges that need to be addressed. The thickness has to be well optimized because efficiency drops as radial NWs become thicker. Also, radial p-n junction can easily become fully depleted in case the doping levels are not high enough. [101]

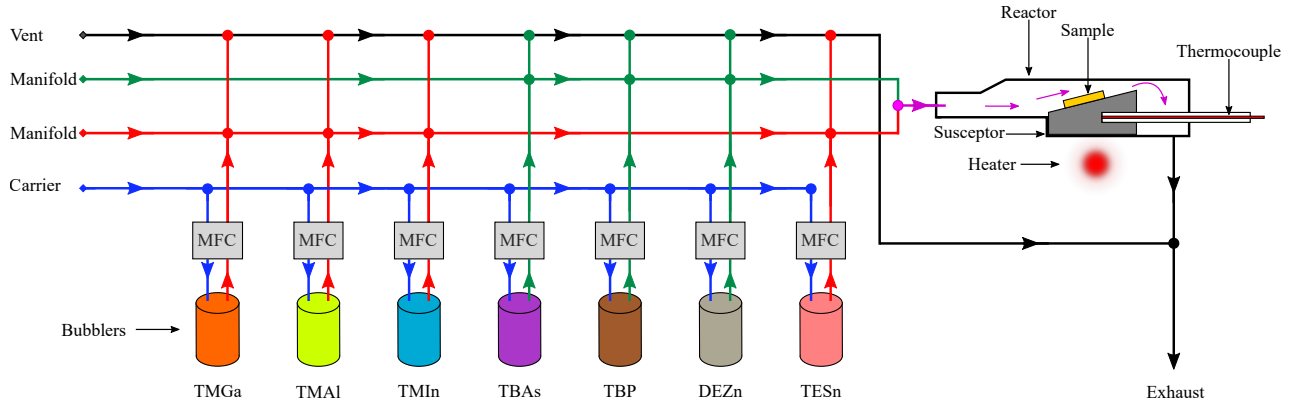
## Chapter 4

# Experimental methods

This chapter describes nanowire solar cell and photodetector fabrication and characterization methods exploited in this work. First, section 4.1 presents metalorganic vapour phase epitaxy (MOVPE) that was used to grow radial p-n junction nanowires. Spin-on glass (SOG) was used as part of the shell-substrate isolation technique described in section 4.2. Further, sections 4.4-4.6 discuss electron beam lithography (EBL), evaporation, lift-off and etching methods that were used to create metal contacts to single nanowires. Nanowires were inspected with scanning electron microscope (SEM) and transmission electron microscope (TEM) described in section 4.3. Finally, section 4.7 presents optical and electrical measurement techniques that were used to characterize the single nanowire device.

### 4.1 Metalorganic vapour phase epitaxy

MOVPE is one of the dominant techniques for NWs synthesis. MOVPE uses vapour phase organometallic source materials that decompose at certain conditions and allow epitaxial crystal growth in controlled manner. Crystal growth process in MOVPE involves many complex processes mostly governed by thermodynamics and kinetics. All nanowires used in this work were grown by atmospheric pressure MOVPE apparatus manufactured by Thomas Swan & Co. Ltd and located at the Micronova Nanofabrication Centre of Aalto University. Figure 4.1. presents the principal schematic of the device. MOVPE system consists of growth reactor chamber, load lock and glovebox, system of ventilation and manifold lines, bubblers with precursors, mass flow controllers (MFC), sensors, valves and control equipment that can be used either manually or automatically via software program.



**Figure 4.1:** Schematic illustration of metalorganic vapour phase epitaxy (MOVPE) apparatus that was used in this work. The arrows on diagram represent the direction of the gas flow. Mass flow controllers (MFC) control the flow of hydrogen carrier gas through the bubblers that contain metalorganic precursors. Saturated gas is directed to the reactor via the system of gas lines. Inside the reactor, samples are placed on the graphite susceptor, which is heated with infrared halogen lamp, and temperature is measured with thermocouple. Group III and group V precursors have separate manifold lines to avoid pre-reactions. By-products are disposed into gas scrubber via ventilation lines.

The metalorganic precursors are stored in steel bubblers in liquid or in solid state. Bubblers are kept at controlled temperatures inside liquid baths that contain water or glycol because each precursor has specific conditions to achieve suitable vapour pressure. Precursors are effectively carbon compounds, hydrogen, and group III or group V atoms. There are various precursors available for MOVPE growth depending on the materials needed such as trimethylindium (TMIn), trimethylaluminum (TMAI), tertiarybutylphosphine (TBP), tetraethyltin (TESn) etc. Therefore, the growth of binary and ternary compound semiconductors is possible. For this work, group III trimethylgallium (TMGa) and group V tertiarybutylarsine (TBAs) were used as sources of gallium (Ga) and arsenic (As) while diethylzinc (DEZn) and disilane ( $\text{Si}_2\text{H}_6$ ) were used for p-type and n-type doping of nanowires respectively.

Hydrogen acts as an inert high-purity carrier gas and it is directed into bubblers via the system of manifolds. Nitrogen is used to flush the lines and the reactor during samples loading. Mass-flow controllers (MFC) control the carrier gas flow to the bubblers where hydrogen saturates with precursor materials. MFCs also control the output gas flow (measured in SCCM) as

well as dilution of saturated gas with hydrogen if needed. Make-up lines always keep the total gas flow constant. Group III and group V precursors have separate manifold lines to avoid unwanted reactions before the reactor. Uniform growth is achieved because of the tilted surface of the susceptor and special reactor shape that creates laminar flow of precursor gases.

All nanowires used in this work were grown on GaAs (111)B substrates. The preparation procedure includes cleaning in ultrasonic bath with isopropanol (IPA) and acetone, followed by deionized water rinse, PLL (Poly-L-Lysine) application for better nanoparticle adhesion and finally colloidal Au nanoparticle (NP) solution deposition to be used as a catalyst. Prepared samples are first placed inside the glovebox and then onto the graphite susceptor inside the reactor. The susceptor should be baked at 750 °C for 10 min without samples each time after it was out of the reactor for more than a few hours. This is done to remove the contamination. The glovebox has a constant nitrogen flow in order to protect the reactor from outside environment and to eliminate any contamination and leakage risks. The actual growth takes place inside quartz reactor at atmospheric pressure. Since the reactor must be tightly shut, a series of underpressure and overpressure tests is performed to ensure that there are no leaks.

The susceptor and samples are heated with infrared halogen lamp and the temperature is measured with thermocouple, which is placed inside the susceptor and protected by the quartz tube. However, temperature readings are generally higher than the actual substrate surface because of the cooling effect of the constant gas flow and thermal conductivity of the susceptor material. The growth temperatures mentioned in this work are thermocouple readings. Usually before the growth starts, substrates are annealed at 650 °C to remove the native surface oxide. During growth, the precursors pyrolyse (or decompose) to release the group III and group V elements which then diffuse and desorb onto the heated sample substrate inside a reactor resulting in NWs growth. The growth temperatures are usually in the range from 400 °C to 650 °C. Unused precursors, toxic by-products and gases are flushed to ventilation lines that are connected to the gas scrubber.

Nanowires synthesis is controlled stepwise by software, which is programmed in the form of algorithms or recipes. Recipe defines the duration of each step, growth temperature, carrier and precursor gas flows, precursor ratios and dilution. Table 4.1 presents a principal recipe which was used for cs-NWs growth in this work.

**Table 4.1:** Main steps of the cs-NWs growth recipe used in this work.

	#	Step	Time (s)	Temp. (°C)	TMGa	TBAs	DEZn	Si <sub>2</sub> H <sub>6</sub>
Core growth	1	Stabilize	300	-	Vent	Vent	Vent	-
	2	Bake	600	650	Vent	Vent	Vent	-
	3	Cooling	-	465	Vent	Vent	Vent	-
	4	Growth	75	465	Reactor	Reactor	Reactor	-
	5	Cooling	-	250	Vent	Vent	Vent	-
	6	Flush	300	-	Vent	Vent	Vent	-
Growth interruption and SOG application								
Core regrowth	1	Stabilize	300	-	Vent	Vent	Vent	Vent
	2	Bake	600	650	Vent	Vent	Vent	Vent
	3	Cooling	-	465	Vent	Vent	Vent	Vent
	4	Growth	75	465	Reactor	Reactor	Reactor	Vent
Shell growth	5	Stabilize	-	-	Vent	Reactor	Vent	Vent
	6	Heating	-	650	Vent	Reactor	Vent	Vent
	7	Growth	10	650	Reactor	Reactor	Vent	Reactor
	8	Cooling	-	250	Vent	Reactor	Vent	Vent
	9	Flush	300	-	Vent	Vent	Vent	Vent

Different parameters such as temperature, time, molar flow ratios and V/III ratio have been varied to achieve the best cs-NW geometry, carrier concentrations and density. The optimized parameters for the particular MOVPE apparatus used in this work are based on previous research and experience of the nanowire research group at Department of Micro- and Nanosciences of Aalto University [10, 57, 102–106]. The recipe starts with 300 s step where all precursors are directed to vent line in order to stabilize the flow, temperature and pressure. During the next step, samples are baked at 650 °C for 600 s under hydrogen flow to remove native oxide and contaminations and to alloy the Au particles with the surface of the substrate. After cooling down to the target temperature of 465 °C and stabilizing the flows, precursor gases are directed into the reactor and core growth commences. During this step DEZn is used as a p-type dopant while TMGa and TBAs are used as sources of gallium and arsenic. In this work, unless stated otherwise, TMGa flow of 10.71  $\mu\text{mol}/\text{min}$ , TBAs flow of 270  $\mu\text{mol}/\text{min}$  and DEZn flow of 0.42  $\mu\text{mol}/\text{min}$  were used for initial core synthesis. Next, the reactor is cooled down to 250 °C. Usually TBAs flow is kept on during cooling in order to avoid nanowire decomposition and As desorption from the surface [107, 108]. However, in case of cs-NW synthesis, it is important to turn

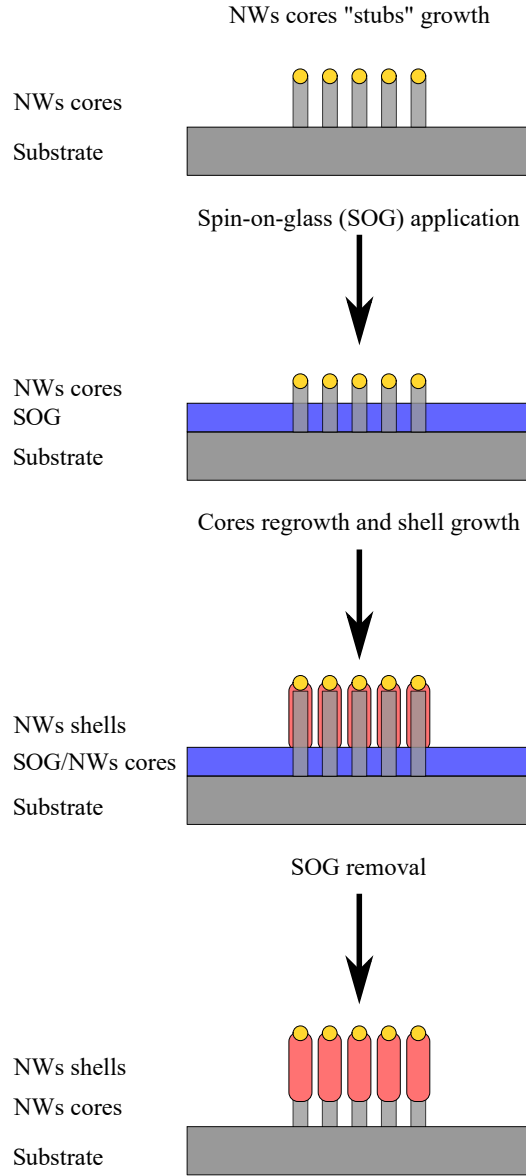
off TBAs flow into the reactor right after the core growth to prevent Ga depletion from the Au seed during cooling step. Otherwise the core will not resume its growth in the same direction during the second MOVPE run [109]. Generally, the last step is flushing of the reactor with hydrogen flow for 300 s.

After the first MOVPE run, the growth is interrupted and spin-on glass layer is applied ex situ as part of the shell-substrate isolation technique which is described in section 4.2. Similar to the first MOVPE run, the second run starts with stabilization and baking. After cooling and stabilization, the core resumes its growth until it reaches its final length. Same growth parameters as in the first MOVPE run are used in this step to ensure pristine quality of the core. Next, the flows are stabilized and reactor is heated up to the target temperature of 650 °C. During 10 s shell growth TMGa flow of 6.43  $\mu\text{mol}/\text{min}$ , TBAs flow of 522  $\mu\text{mol}/\text{min}$  and  $\text{Si}_2\text{H}_6$  flow of 5 sccm were used. Finally, the reactor is cooled down and flushed. The nominal V/III ratio for the core and shell growth was 25.

## 4.2 Nanowire shell-substrate isolation technique

Radial p-n junction GaAs NWs samples for this work were fabricated using lithography-free shell-substrate isolation technique invented by nanowire research group at Department of Micro- and Nanosciences of Aalto University [109]. The method is based on two step MOVPE growth interrupted by application of the insulating spin-on glass (SOG) layer between the steps that effectively isolates core and shell. The technique is simple, fast, and reliable: it does not require multiple lithography and etching steps to expose the core as other shell-substrate isolation methods [110–113].

SOG used in this work was ACCUGLASS T-312B and T-512B provided by Honeywell. Figure 4.2 shows the basic steps of the isolation technique. First, axial NW cores are synthesized in MOVPE. These “stubs” have roughly half of the length of the final nanowire. The growth process is interrupted and samples are removed from the reactor to the lab environment. Next, SOG is spin coated at 1000 RPM for 20 s forming an isolating layer of 1  $\mu\text{m}$  to 2  $\mu\text{m}$ . After that, samples are baked using hot plate with sequential temperature increase from 80 °C to 250 °C in 3 steps 60 s bake time each. This is to allow gradual solvent evaporation.



**Figure 4.2:** Schematic drawing of the nanowire shell-substrate isolation technique. Axial NW cores are grown in the first MOVPE step. The growth is interrupted and SOG is applied to cover part of the cores. NW cores are further regrown and radial NW shells are wrapped around the cores in the second MOVPE step. Finally, SOG is etched in hydrofluoric acid (HF) resulting in core-shell nanowires.

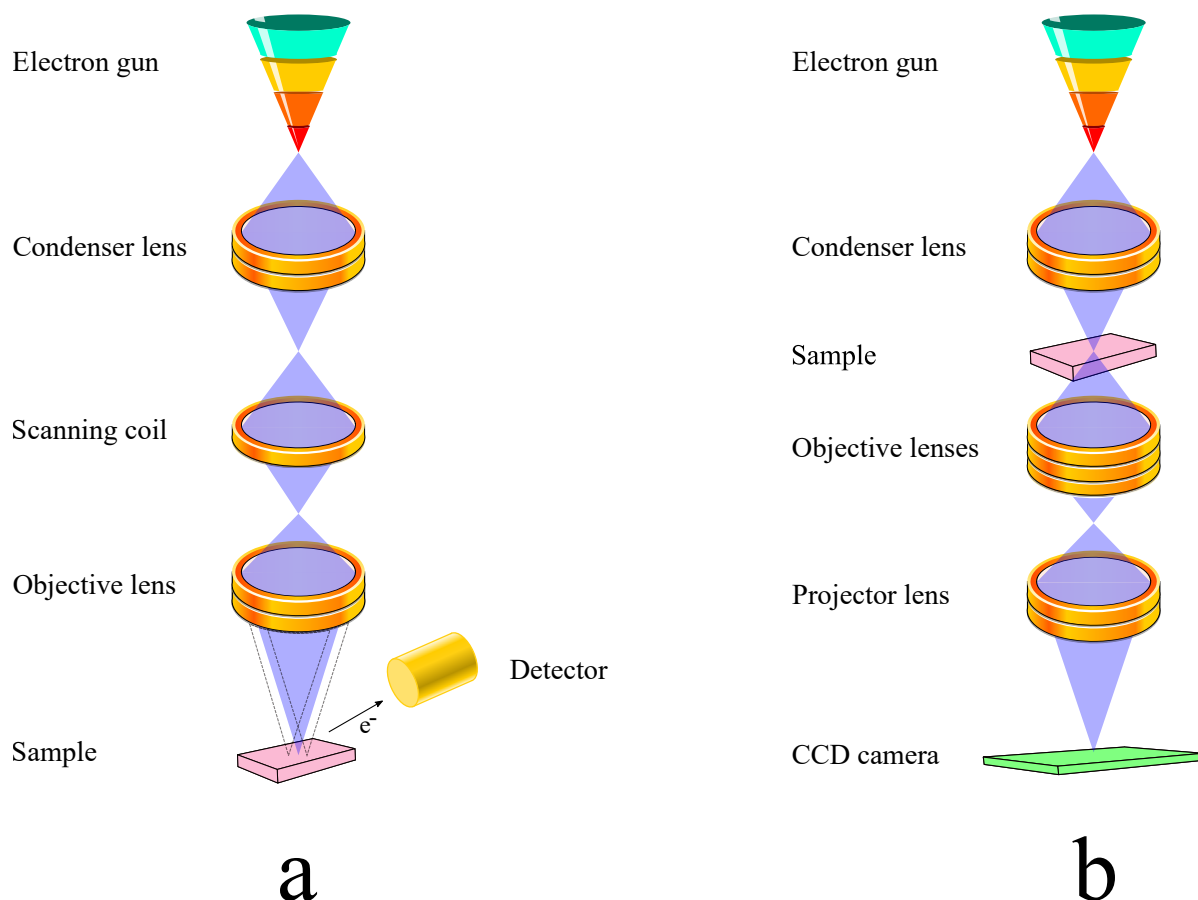
Further, samples are cured in furnace at 425 °C for 1 h in nitrogen atmosphere. Temperature starts at 300 °C and ramps up to 425 °C at a rate



of  $2.5^{\circ}\text{C}/\text{min}$ , remains at  $425^{\circ}\text{C}$  for 1 h and then ramps down at a rate of  $5^{\circ}\text{C}/\text{min}$ . This is followed by the second MOVPE step where samples are first annealed in situ at  $650^{\circ}\text{C}$  under hydrogen flow for 10 min to remove the native oxide and SOG residues. Then NW cores resume the growth to their final length and the radial shells are wrapped on those parts that are not covered by SOG. Finally, SOG is etched in 1:5 mix of HF (50%) and DI water for 60 s. Thus, radial p-n junction cs-NWs with shell-substrate isolation are fabricated.

### 4.3 Electron microscopy

Electron microscopy is one of the widely-used techniques in nanotechnology because it can produce images with resolution down to atomic range and large depth of field, which is applicable to NWs characterization. Morphological properties of the NWs used in this work were inspected using scanning electron microscopy (SEM) while structural properties were examined with high-resolution transmission electron microscopy (TEM). Figure 4.3 (a) shows the principal schematic of SEM. Typical SEM system consists of electron source, a set of condenser lenses, scanning coils and objective lens, sample holder and detectors. The components are installed inside SEM column and operated at vacuum conditions.



**Figure 4.3:** Schematic diagram of main components of (a) scanning electron microscope (SEM) and (b) transmission electron microscope (TEM). In both systems, emitted electrons are accelerated, shaped into an electron beam, focused and scanned over the sample. In SEM, the image is formed by detecting secondary (SE) or backscattered electrons (BSE) that are created due to interaction of the primary electrons (PE) with the surface of the sample. In TEM, electron beam passes through the sample and the image is formed by detecting the transmitted electrons.

Electrons are emitted from electron source (heated filament) and accelerated by high electric field. Commonly used acceleration voltage range is 1 kV to 30 kV. Condenser lenses shape the accelerated electrons into electron beam, which is focused and demagnified down to nanometer size spot by objective lens. The position of the spot is controlled with scanning coil that deflects the beam and scans the electron probe in a raster over the surface of

a sample. When the incident or primary electrons (PE) hit the sample, several signals are generated including secondary electrons (SE), backscattered electrons (BSE), X-rays and Auger electrons. [114, p. 1-5]

Usually only SE and BSE collected by detectors are used to form an SEM image. SE are produced because of inelastic scattering of PE from very thin (few nanometers) surface layer of the sample. BSE result from almost elastic scattering of PE from much greater depths of the specimen. The image is created by detecting the signal at each position of the electron beam spot by raster scanning with certain time intervals. Different spots on the sample produce variations in intensity of the signal, which is used to form a contrast greyscale image of the surface topography. [114, p. 1-5]

All samples fabricated in this work were studied using SEM Zeiss Supra 40 located at the Micronova Nanofabrication Centre of Aalto University. System has Schottky field emitter and can obtain images with resolution of up to 0.8 nm at 30 kV. SEM was operated at 5 kV with the in-lens detector and working distances of 2 mm to 4 mm, which was optimal to eliminate the charging effect, and at the same time not to destroy the NWs due to high energy of the beam. The device was used for characterization of NWs dimensions, morphology, distribution, and density at each step during the radial p-n junction fabrication as well as for inspection of the final single nanowire solar cell prototype.

Figure 4.3 (b) shows the principal schematic of TEM that has a similar structure to SEM. The main difference is that TEM can reach atomic resolution since it uses much higher acceleration voltages (normally 100 kV to 200 kV) that allow electron beam to pass directly through the sample, which is placed before the objective lenses. This puts a limit on sample thickness that must be less than a few hundred nanometers. However, it is not a problem for nanowires that have nanoscale diameter. The detector (typically CCD camera) collects the transmitted signal to acquire atomic resolution images, electron diffraction patterns and lattice periodicity of the crystal. [115, p. 5-7]

Energy-dispersive X-ray spectroscopy (EDX) is a technique in electron microscopy that allows to perform chemical characterization of material. It is based on detection of characteristic X-rays that are emitted after outer shell electron replaces the electron in the inner shell which was prior ejected by the incident high energy electron beam. Since characteristic X-rays correspond to the energy difference between outer and inner shells of the atom, they are unique for different elements. It must be said that the detection and interpretation of the EDX spectra can be demanding as many energy levels are located close to each other. [115, p. 365-367]

NWs grown in this work were studied using TEM JEOL JEM-2200FS

operated at 200 kV and located at the Nanomicroscopy Center of Aalto University. The device was used for characterization of NWs crystal structure and crystal quality. TEM samples were prepared by mechanical dispersion of NWs onto commercially available TEM copper grids covered with a holey carbon film. Additionally, EDX was performed for elemental analysis of NWs studied in TEM.

## 4.4 Electron beam lithography

Electron beam lithography (EBL) operation is based on the same principles as SEM and TEM. In EBL, finely focused Gaussian round electron beam is used to expose custom predefined patterns on electron-sensitive resist that is spin coated on the surface of the specimen. Apart from blanker and advanced deflection system for moving the beam, EBL has a very similar structure and components to SEM. Blanker acts as a shutter and turns the electron beam on and off, hence, exposing only certain areas depending on the pattern. Extremely high resolutions below ten nanometers can be easily achieved without any need for photomasks as in traditional UV photo lithography. [116, p. 142-143] However, the main limitations of EBL are exposure speed and throughput as it takes impractically long time to write high resolution patterns and whole wafers. What is more, EBL systems can be very expensive with the prices of over few million euros. This makes EBL unfeasible for industrial production but exceptional for rapid prototyping, device fabrication on a nanometer scale, research and development. [117, p. 95-96]

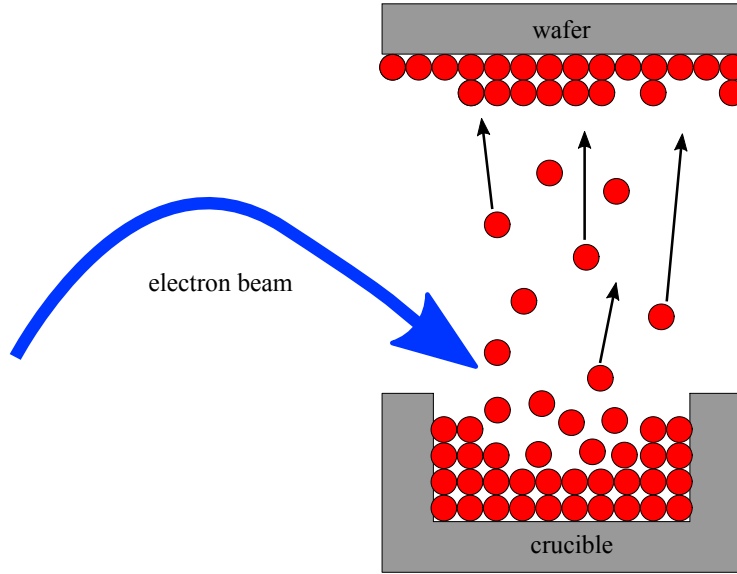
Sample preparation starts with spin coating of e-beam resist which is usually a high molecular-weight polymer dissolved in a liquid solvent. Spin coating is done using a spinner with the spinning speed of few thousand revolutions per minute that effectively forms a uniform thin layer and, together with resist concentration, determines the final thickness. There are two types of resists: positive and negative. In positive resist, exposed areas are dissolved away in developer as long polymer chains are cut by the electron beam. In negative resist, exposed areas are strengthened due to crosslinking that leads to reduced solubility. Resist spin coating is followed by soft baking at temperature ranging from 130 °C to 180 °C to evaporate the remaining solvent. [116, p. 144-146]

For this work all the individual contacts to single nanowires were fabricated using EBL Vistec EPBG5000pES system located at the Micronova Nanofabrication Centre of Aalto University. The system was operated at 100 kV with maximum pattern generator frequency of 50 MHz and expose dose of 1000  $\mu\text{C}/\text{cm}^2$ . Polymethyl methacrylate (PMMA) on the top layer

and methyl methacrylate (MMA) on the bottom layer were used as positive resists for a standard double-layer stack. Low molecular weight MMA copolymer was used to obtain higher sensitivity relative to high molecular weight PMMA and to create an undercut profile crucial for high resolution lift-off technique. A 1:3 solution of methyl isobutyl ketone (MIBK) and isopropanol (IPA) was employed as a developer for selective removal of resist. LayoutEditor software was utilized to design the patterns of the contacts to single nanowires. BEAMER software environment was used for layout data preparation and its conversion to machine formats readable by EBL apparatus.

## 4.5 Evaporation and lift-off

Evaporation is a classical thin-film physical vapour deposition (PVD) technique that is commonly used in microfabrication. Figure 4.4 shows the schematic of the electron beam evaporation process. Electron beam gun is used to heat solid target to high temperatures so that the material is evaporated and deposited on the substrate surface. High vacuum (HV) or ultra-high vacuum (UHV) conditions with pressure range of  $10^{-5}$  torr to  $10^{-11}$  torr are required for particles to travel directly onto the specimen without colliding with the background gas. [117, p. 48-49]



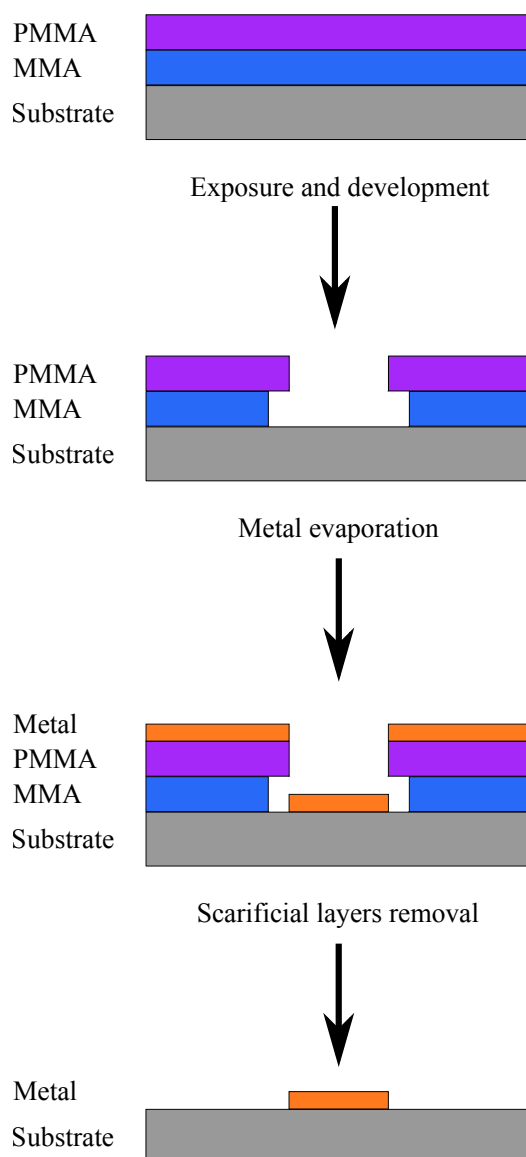
**Figure 4.4:** Schematic illustration of electron beam evaporation process. Electron beam gun heats the target material to high temperatures inside the crucible. As a result, the material evaporates directly onto the substrate. System is operated under high vacuum conditions.

Typical deposition rates for evaporation are 0.1 nm/s to 1 nm/s which is relatively low comparing to other thin film deposition techniques. Furthermore, evaporation has a poor step coverage and uniformity. However, the method is not as expensive but versatile as a variety of metals and even dielectrics can be deposited at almost room temperature which makes it suitable for rapid prototyping and R&D.

For this work metal contacts to single nanowires were evaporated using Edwards E306A system located at the Micronova Nanofabrication Centre of Aalto University. The metal stacks used to p and n-type GaAs NWs contacts are widely used and reported to give best ohmic behaviour [118, 119]. For contacts to Zn doped p-type cores,  $\text{Au}_{95}\text{Zn}_5$  alloy was used with evaporation rate of 0.1 nm/s to 0.2 nm/s and total thickness of 115 nm. For contacts to Si doped n-type shells,  $\text{Ni}/\text{Au}_{88}\text{Ge}_{12}/\text{Ni}$  alloy was used with evaporation rate of 0.1 nm/s to 0.2 nm/s and total thickness of 5 nm/115 nm/15 nm. Rapid thermal annealing tool was utilized to anneal the n-contact metal at 320 °C in  $\text{N}_2$  for 60 s.

Lift-off is a general method of deposited film patterning using sacrificial material. It is mostly employed for fabrication of metallic interconnections. Figure 4.5 presents a typical lift-off process flow. First, resists (in this case

MMA and PMMA) are spin coated on the surface of the sample and the pattern is exposed by means of EBL or photolithography. As was previously mentioned, MMA copolymer is used together with PMMA to achieve an undercut profile and avoid metal sidewalls (“ears”) on the edges. After the resist development in MIBK:IPA 1:3 solution, target material is deposited using evaporation covering the whole surface of the sample including the exposed areas. Finally, sacrificial resist layer and evaporated film on top of it are stripped away with solvent remover (in this case acetone) leaving the metal film only on those areas which were initially exposed. [117, p. 289-290]

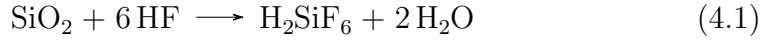


**Figure 4.5:** Schematic illustration of lift-off process. Sacrificial resists (MMA and PMMA) are deposited on the sample and patterned using EBL. Undercut profile is created after resist development due to combination of two resists that have different molecular weight. This prevents forming of the metal sidewalls on the edges of the pattern. Metal thin film is evaporated over the sample. Resists and unwanted metal are removed in solvent leaving the metal at only unprotected areas.



## 4.6 Etching

Etching is a process of removing a material that is not protected with mask by eroding it either chemically or physically. Etching is an essential and critical step in most of the microfabrication processes. Resist is commonly used as a mask for etching in photolithography and EBL, though more durable thin film layers of silicon nitride ( $\text{SiN}_x$ ), silicon dioxide ( $\text{SiO}_2$ ) or metals could be employed as mask materials. There are two main types of etching: wet etching and dry (plasma) etching, often referred to as reactive ion etching (RIE). Wet etching uses liquid chemicals such as acids while dry etching relies on reactive gases. [117, p. 127-128] For example, basic reaction of  $\text{SiO}_2$  wet etching with HF is given by



The chemical reaction was used in this work during wet etching of SOG layer. Basic reaction of  $\text{SiO}_2$  plasma etching with gaseous etchant is as follows

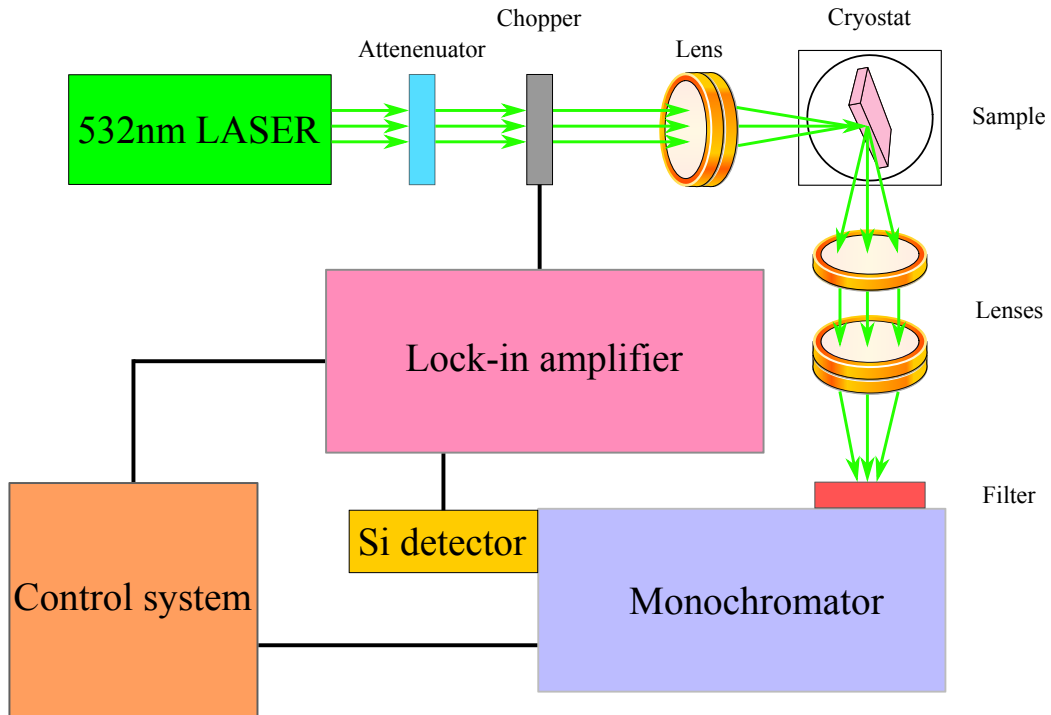


There are two different etching profiles that can be achieved by applying either dry or wet etching. Most wet etchants produce generally undesirable isotropic etching (undercutting) profile which, however, can be tuned depending on etchant concentration and temperature. On the contrary, RIE can produce anisotropic etching profile with almost vertical sidewalls, crucial for complex structures. [117, p. 128-130]

## 4.7 Optical and electrical characterization

Photoluminescence (PL) is a non-destructive spectroscopy method that is used for characterization of optical properties of semiconductors. PL is one of the key characterization techniques for NWs research because it can provide information about band gap transition energy, material composition, surface properties, crystal structure and transitions arising from impurities or defect states. In PL, incident laser beam excites electrons from valence band to conduction band and the electrons recombine either radiatively or non-radiatively. Photons are generated as a result of radiative recombination and their energy corresponds to the band gap of the material. In order for electrons to be excited to higher states, laser wavelength must be smaller than the wavelength corresponding to the band gap of the specimen. Furthermore, PL results can be greatly affected by the power density

of the excitation source as well as measurement temperature. It is common to perform power dependency measurements that can reveal additional details about optical properties as e.g. impurity states can saturate at higher excitation power. Moreover, low temperature (LT) PL measurements can provide clearer results and higher intensities as photons are generated from excitons rather than electron-hole recombination while a thermal excitation and phonon interaction are effectively suppressed.



**Figure 4.6:** Schematic diagram of the PL setup that was used for the optical characterization of NWs.

In this work, NWs optical properties were characterized using PL setup located at the Micronova Nanofabrication Centre of Aalto University. Figure 4.6 shows the schematic illustration of the apparatus. Frequency doubled Nd:YVO<sub>4</sub> laser with a wavelength of 532nm was used for excitation. The beam was focused on the sample and the emitted light was collected by the monochromator. The attenuator was used to reduce the excitation power to required level and the chopper was used to modulate the intensity of light. A filter with cut-off wavelength of 610nm was placed before the monochromator in order to block the actual laser signal. The Si detector, located at the output of the monochromator, was used to measure the intensity of

transmitted light. The lock-in amplifier was used to amplify the signal which was then collected and processed by the software. The closed cycle cryostat with liquid-helium cooling was used for low temperature PL measurements (down to 10 K).

The photocurrent measurements were carried out using custom setup located in the same premises. First, the polychromatic light from xenon arc lamp source was directed to the entrance slit of the monochromator. Next, the monochromatic light after the monochromator was fed to a set of mirrors, lenses and the chopper, then guided through the multi-mode fiber and finally focused on the actual sample. The custom microscope with a web camera was used to monitor the position of the sample and needle probes contacts. The lock-in amplifier was used to measure the electrical response signal of the sample, and the source measure unit instrument was used to bias the sample. During the spectrum scan, the monochromator grating was changed to higher groove density grating at 800 nm for optimal diffraction efficiency and the filter with cut-off wavelength of 610 nm was used to cut out the higher order diffraction peaks of shorter wavelengths that spatially overlap with the first order peaks of longer wavelengths. As a result, the total spectral range of operation was from 400 nm to 1100 nm.

A slightly modified setup was used for the power normalized measurements. In particular, the incoming light was split into two with a 50:50 beam splitter after the fiber. First part went directly to the pyroelectric detector to be used as the power reference and the other part went to the sample. The flat band pyroelectric detector was used as it has no spectral dependence. The detector was connected to the first lock-in amplifier and the sample signal was collected by the second lock-in amplifier. Both amplifiers used the same chopper signal. The amplified signal from the pyroelectric detector was fed to the auxiliary port of the second lock-in amplifier. Finally, the amplified signal from the sample was divided with signal from auxiliary port. The ratio calculation was done automatically in the second lock-in amplifier.

Electrical measurements are important part of device characterization. Current-voltage (I-V) characteristics are obtained by scanning the desired bias voltage range across the device and measuring the corresponding current. In this work, I-V characteristics of the p-n junctions as well as metal-semiconductor ohmic contacts were acquired using Karl Süss Probe station equipped with HP 4155A semiconductor parameter analyzer. Microscope and needle probes with fine positioning adjustment were used to contact the single nanowire contact pads defined by EBL.

## Chapter 5

# Results and discussion

This chapter describes and elaborates on the results and findings that were obtained during this work. First, section 5.1 explains synthesis of radial p-n junction GaAs cs-NWs. Next, fabrication method of single nanowire solar cells is presented in section 5.2. Section 5.3 discusses optical and electrical characterization results. Finally, section 5.4 presents the crystal structure of radial p-n junction GaAs cs-NWs.

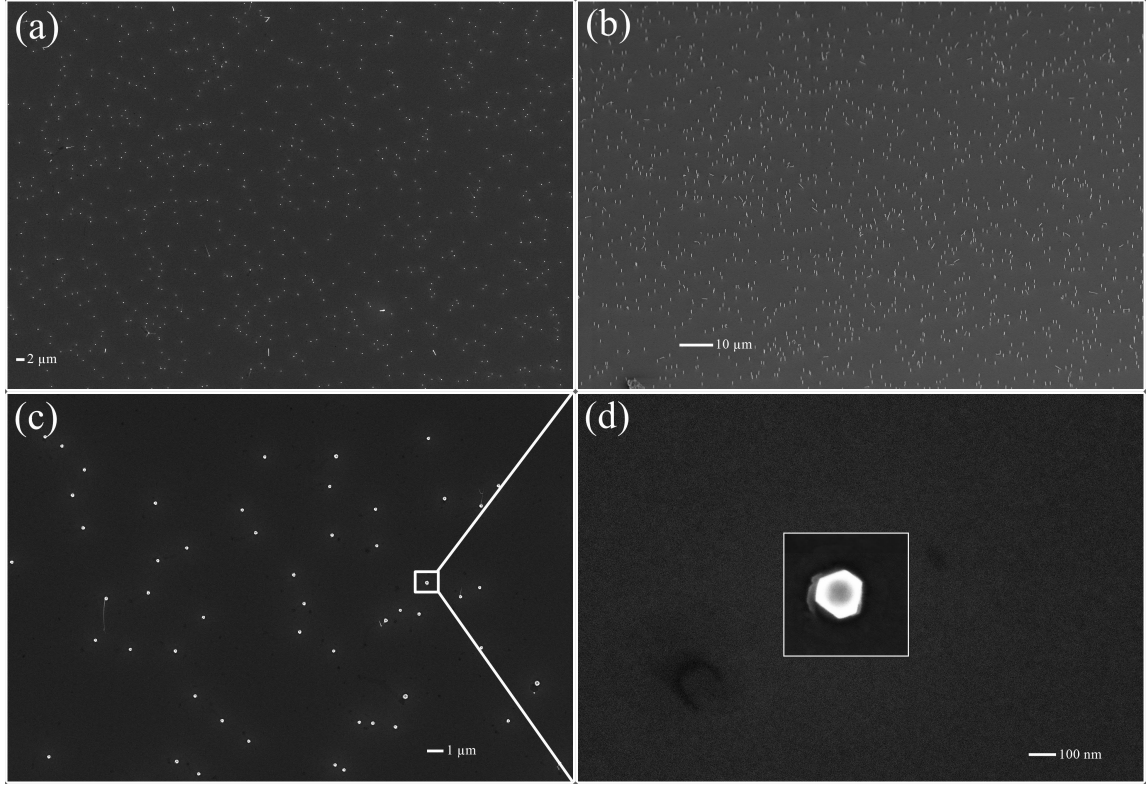
### 5.1 Synthesis of radial p-n junction nanowires

Radial p-n junction core-shell GaAs NWs samples were grown on GaAs (111)B substrates using MOVPE. TMGa and TBAs were used as the gallium and arsenic sources and doping was accomplished with DEZn and Si<sub>2</sub>H<sub>6</sub> for p-core and n-shell growth, respectively. The reactor temperature was 465 °C during the core growth and 650 °C during the shell growth while hydrogen acted as the carrier gas. NWs were grown per growth recipes described in section 4.1.

#### 5.1.1 Nanowire core growth

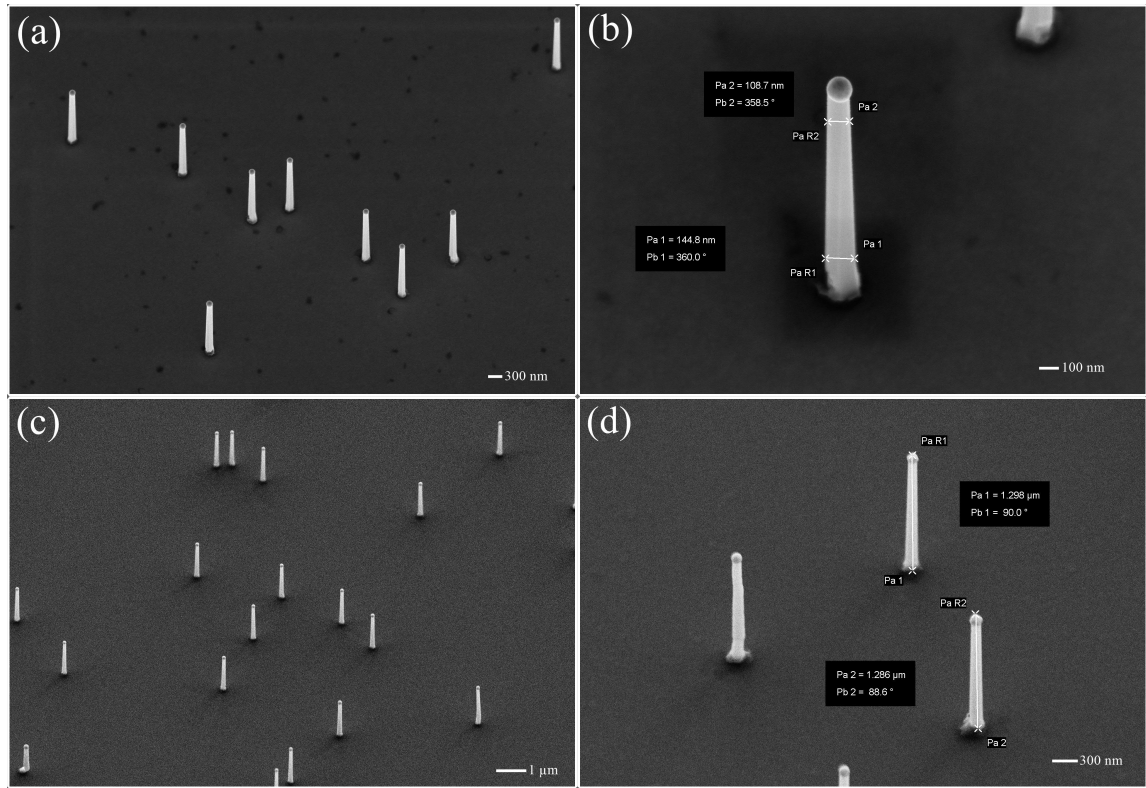
First, samples were cleaned and prepared as discussed in section 4.1. Au NPs with diameter of 100 nm were used as seed material for VLS growth. This was followed by cs-NW growth using shell-substrate isolation technique that was presented in section 4.2. In particular, after NW cores synthesis, the growth process was interrupted and samples were removed from the reactor. Next, SOG was spin coated, samples were baked using hot plate and cured in furnace in nitrogen atmosphere. During the second MOVPE step, NW cores resumed the growth to the final length and radial shells were wrapped

on those parts that were not covered by SOG. Finally, SOG was etched in HF.



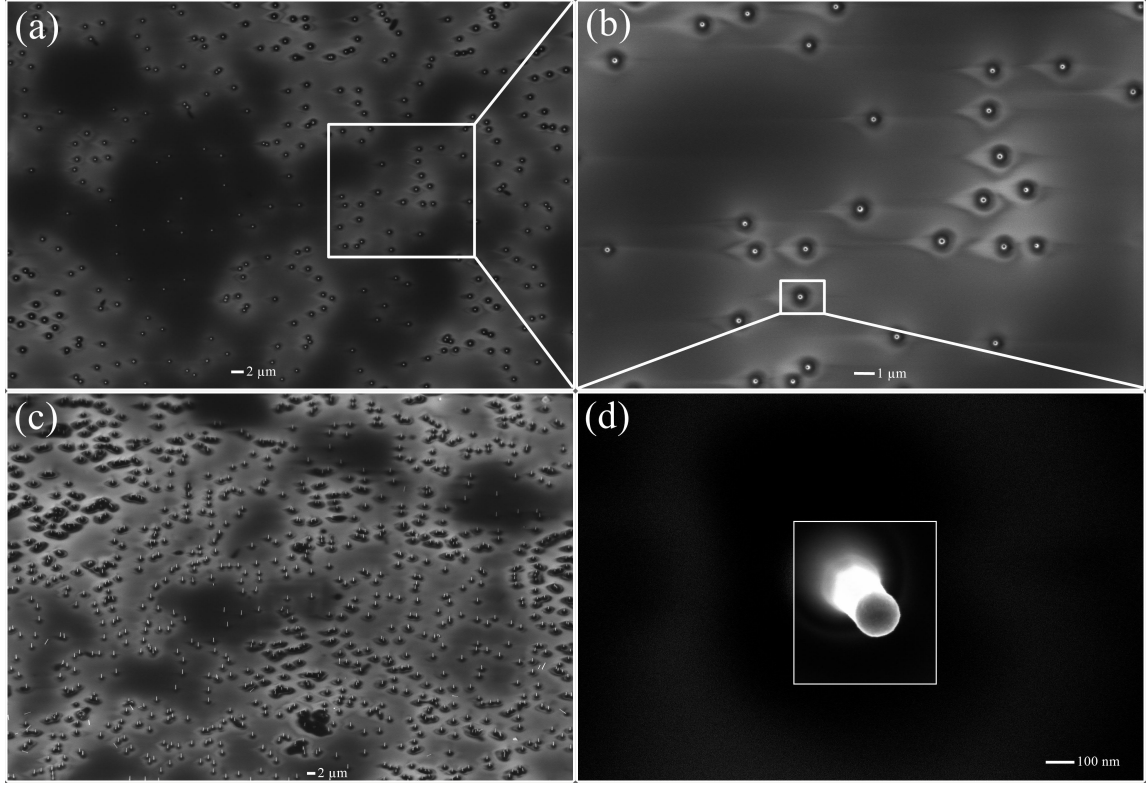
**Figure 5.1:** SEM micrographs of GaAs NW cores grown on GaAs (111)B substrate. Tilt of the image is  $30^\circ$  for (b) and  $0^\circ$  for (a), (c), (d).

Figure 5.1 presents SEM images of GaAs NW cores that were obtained after the first MOVPE run. The growth temperature was  $465^\circ\text{C}$  resulting in predominantly axial growth. The NW density was approximated as  $1 \text{ NW}/\mu\text{m}^2$  which means that there were roughly one million NWs per  $1 \text{ mm}^2$ . Figure 5.1 (d) shows a magnified image of the nanowire tip which clearly indicates that NWs have hexagonal morphology. Figure 5.2 depicts  $30^\circ$  tilted SEM images of the NW cores. As expected, NWs grew in vertical direction and almost no kinking or stacking faults were observed. However, the cores were slightly tapered with tip diameters between 100 nm and 110 nm and base diameters between 140 nm and 150 nm. As can be seen, NWs lengths were between  $2.5 \mu\text{m}$  and  $3 \mu\text{m}$  depending on the location on the substrate. Au catalyst NPs with diameter of 100 nm are clearly visible at the tip of each NW indicating that the growth occurred via the VLS mechanism.



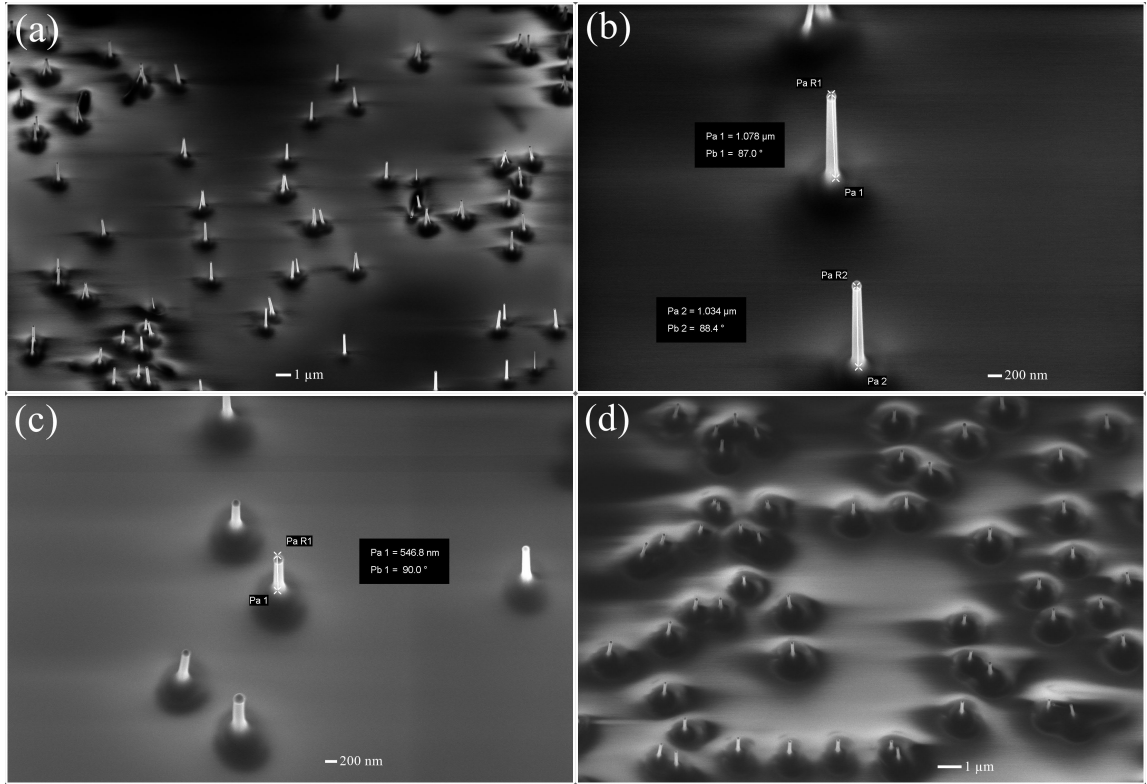
**Figure 5.2:** SEM micrographs of GaAs NW cores grown on GaAs (111)B substrate. Tilt of the images is  $30^\circ$ .

### 5.1.2 Shell-substrate isolation



**Figure 5.3:** SEM micrographs of GaAs NW cores after ex situ application of SOG insulating layer. Inhomogeneous background colour is the result of charging effect due to non-conductive nature of the SOG. Tilt of the image is  $30^\circ$  for (c) and  $0^\circ$  for (a), (b), (d).

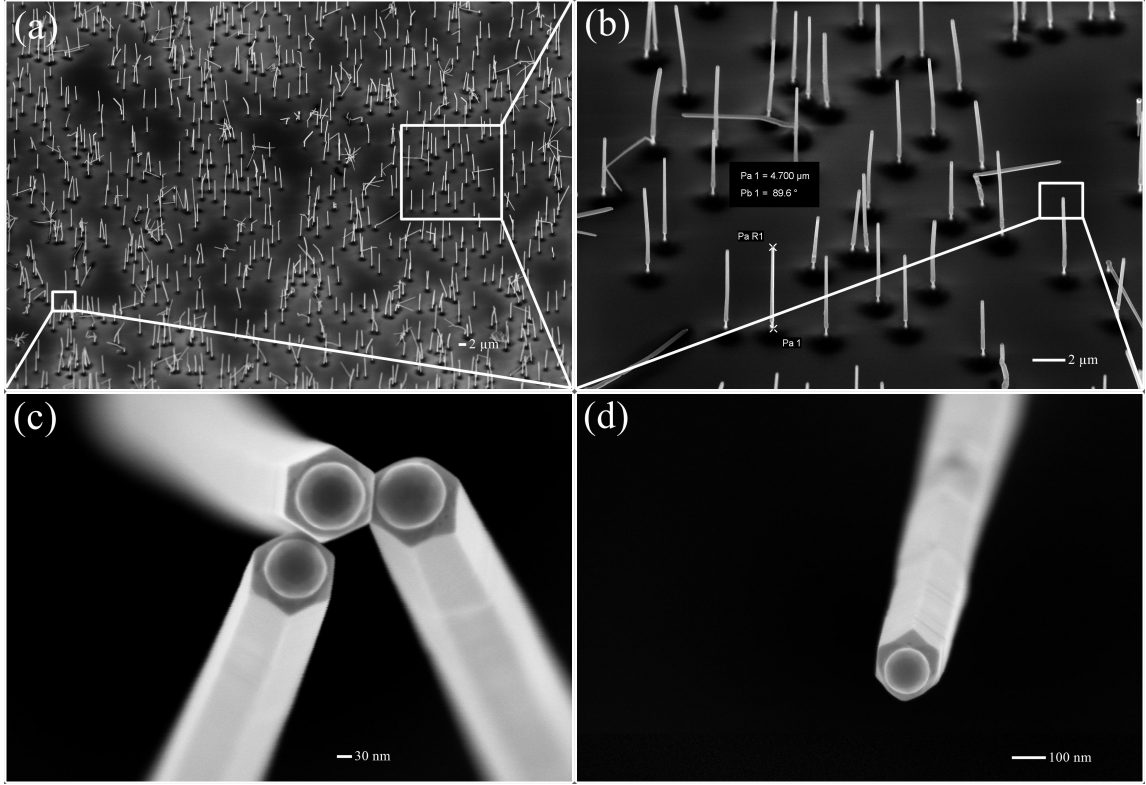
Next step consisted of spin coating of the ACCUGLASS T-512B SOG, sequential hot plate bake and furnace curing in nitrogen atmosphere. Figure 5.3 portrays SEM images of GaAs NW cores after the application of the SOG layer. Apparently, NWs were intact and undamaged after the SOG spin coating. The contrast difference on the SEM micrographs is due to charging of the non-conductive SOG layer. As can be seen from figure 5.4, SOG covered between  $1\text{ }\mu\text{m}$  and  $2\text{ }\mu\text{m}$  of the NW base. Thicker SOG layer was observed near the centre of the sample and thinner near the edges. Nevertheless, SOG layer was smooth and continuous over the area of the whole sample, and no bubbles, a common problem associated with SOG, were noticed.



**Figure 5.4:** SEM micrographs of GaAs NW cores after ex situ application of SOG insulating layer. Tilt of the images is 30°.



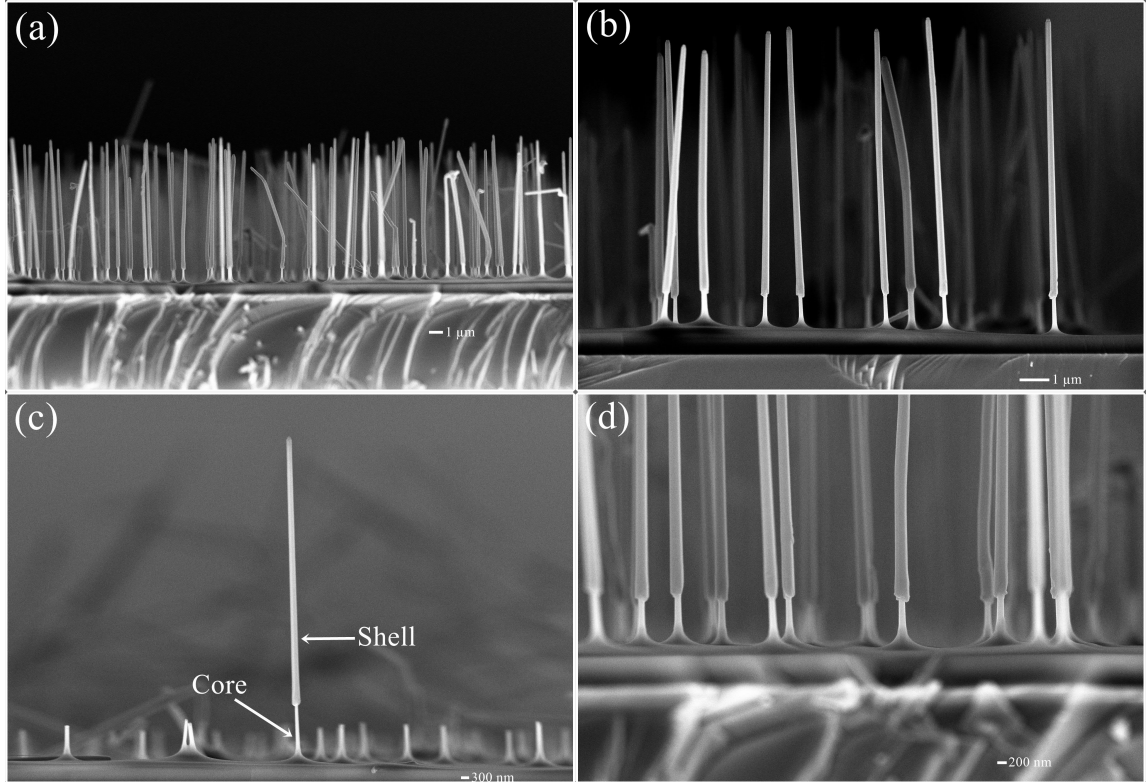
### 5.1.3 Nanowire shell growth



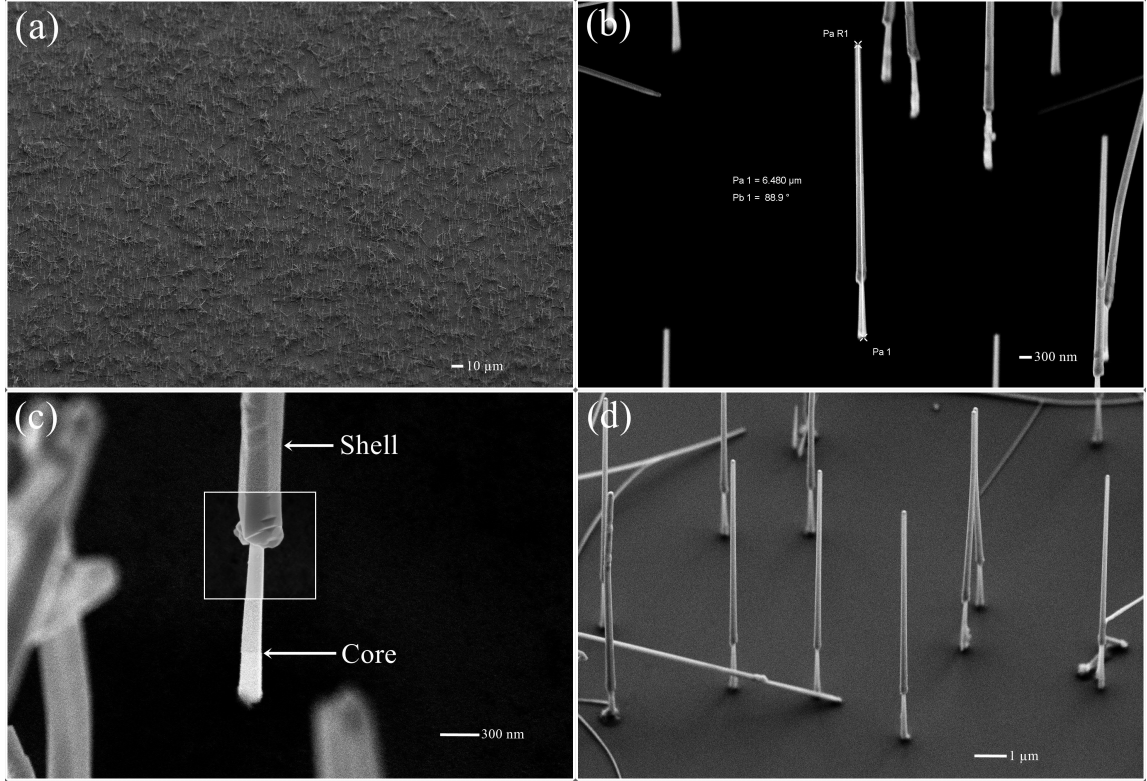
**Figure 5.5:** SEM micrographs of radial p-n junction GaAs cs-NWs after core regrowth and shell synthesis. Tilt of the images is 30°.

At the second MOVPE run the same growth parameters were used to regrow the cores to the final length. Prior to the growth, samples were annealed in situ at 650 °C under hydrogen flow for 10 min to remove the native oxide and SOG residues. Next, radial shells were wrapped around NWs that were not protected by SOG. During this step the growth temperature was 650 °C resulting in predominantly radial growth. Figure 5.5 presents 30° tilted SEM images of radial p-n junction GaAs cs-NWs after the second MOVPE run. Although some NWs changed the growth direction to non-vertical, the majority of NWs resumed the growth vertically. This can be attributed to SOG remnants that were still present on some of the NWs as well as possible local variations of temperature and precursor flows. The average diameter of hexagonal cs-NWs was 150 nm. Moreover, the hexagonal shells and Au catalyst NPs are clearly visible at the NW tips indicating that the core re-

growth and shell growth also occurred via the VLS mechanism. Figure 5.6 shows cross-sectional SEM images of the cs-NWs. Insulating SOG layer on top of the substrate is depicted in figure 5.6 (b). Figure 5.6 (c) also shows an interesting segment where NWs broke off the substrate leaving only core stubs behind.

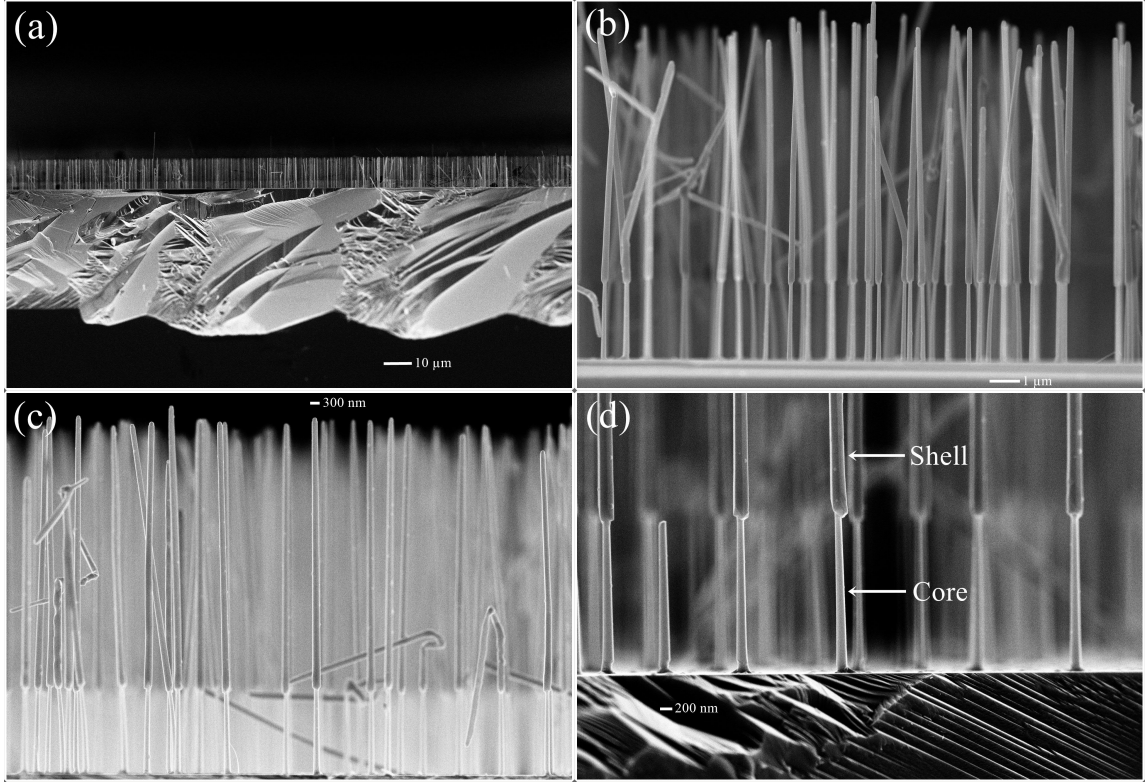


**Figure 5.6:** Cross-sectional SEM micrographs of radial p-n junction GaAs cs-NWs after core regrowth and shell synthesis.



**Figure 5.7:** SEM micrographs of radial p-n junction GaAs cs-NWs after the etching of SOG. Tilt of the images is 30°.

As the last step, SOG layer was etched in 1:5 mix of HF (50%) and DI water. Figure 5.7 depicts 30° tilted SEM images of the final radial p-n junction NWs with shells effectively isolated from the substrate. It has to be said that some NWs were broken during etching, however the number of straight NWs was still considerable. Figure 5.7 (c) shows magnified image of the core-shell interface. The core and shell segments of the NW can be easily distinguished which confirms that the core-shell NWs were formed. Figure 5.8 shows cross-sectional SEM images of the cs-NWs in their final form. As can be seen, very dense, good quality array of cs-NWs was formed. The total NW length varied between 10  $\mu\text{m}$  and 12  $\mu\text{m}$  and the exposed core segments were roughly 2.5  $\mu\text{m}$ .

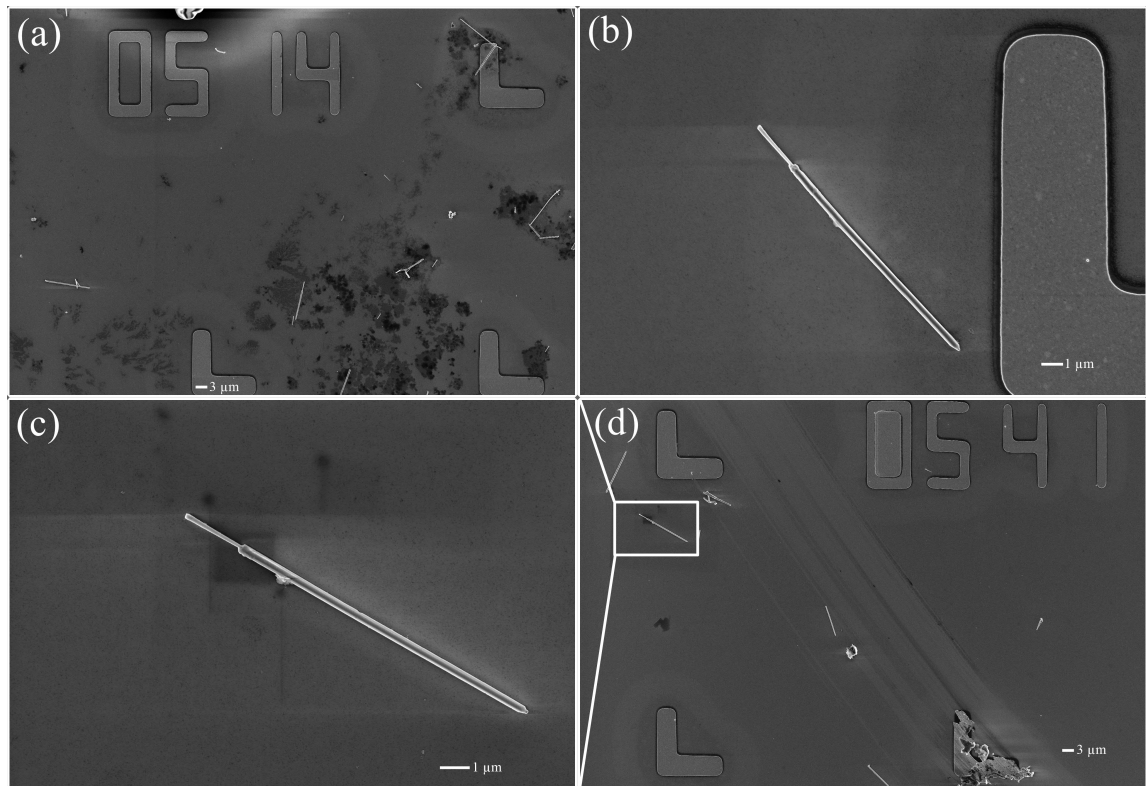


**Figure 5.8:** Cross-sectional SEM micrographs of radial p-n junction GaAs cs-NWs after the etching of SOG.

## 5.2 Fabrication of single nanowire solar cell

### 5.2.1 Dispersion of the nanowires

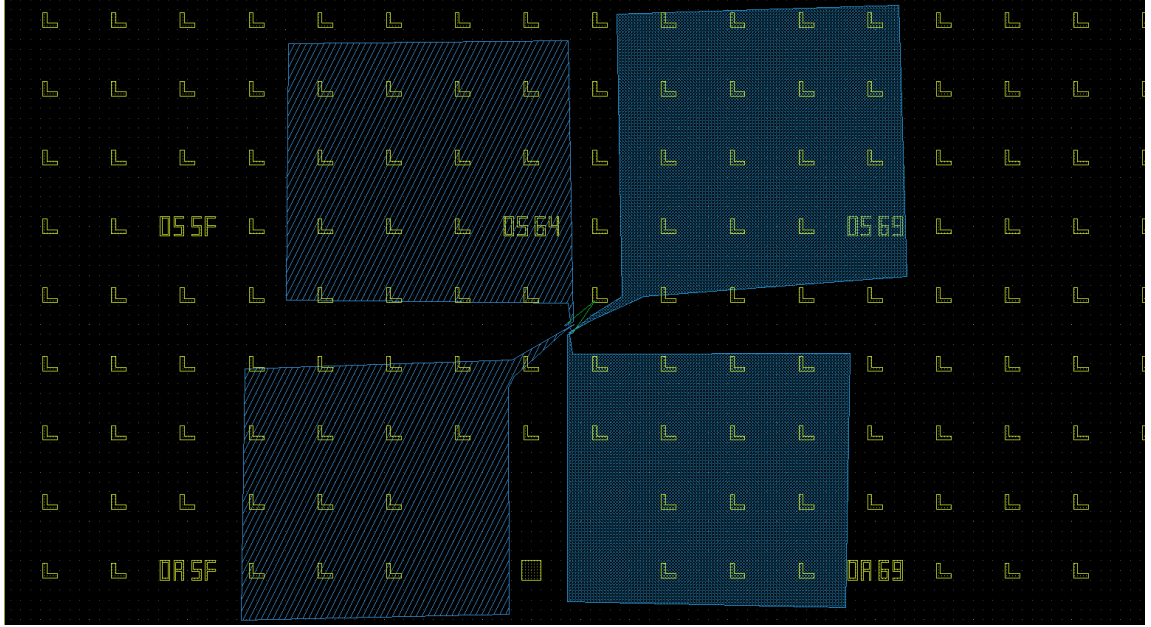
Fabrication of single nanowire solar cell started with dispersion of the NWs onto the  $\text{SiO}_2$  coated Si contact substrates that had predefined alignment markers. The chip size was 1 cm x 1 cm. The dispersion process was initiated by immersing a cleaved piece of NW sample into ethanol and following ultrasonication step. Consequently, cs-NWs were detached from the growth substrate and transferred to the contact substrate by drop casting the ethanol solution that contained the suspended NWs. As a result of liquid evaporation, intact cs-NWs were successfully deposited onto the contact sample. Figure 5.9 presents SEM images of the sparsely scattered GaAs cs-NWs after dispersion.



**Figure 5.9:** SEM micrographs of GaAs cs-NWs after dispersion onto the  $\text{SiO}_2$  coated Si contact substrates with predefined alignment markers.



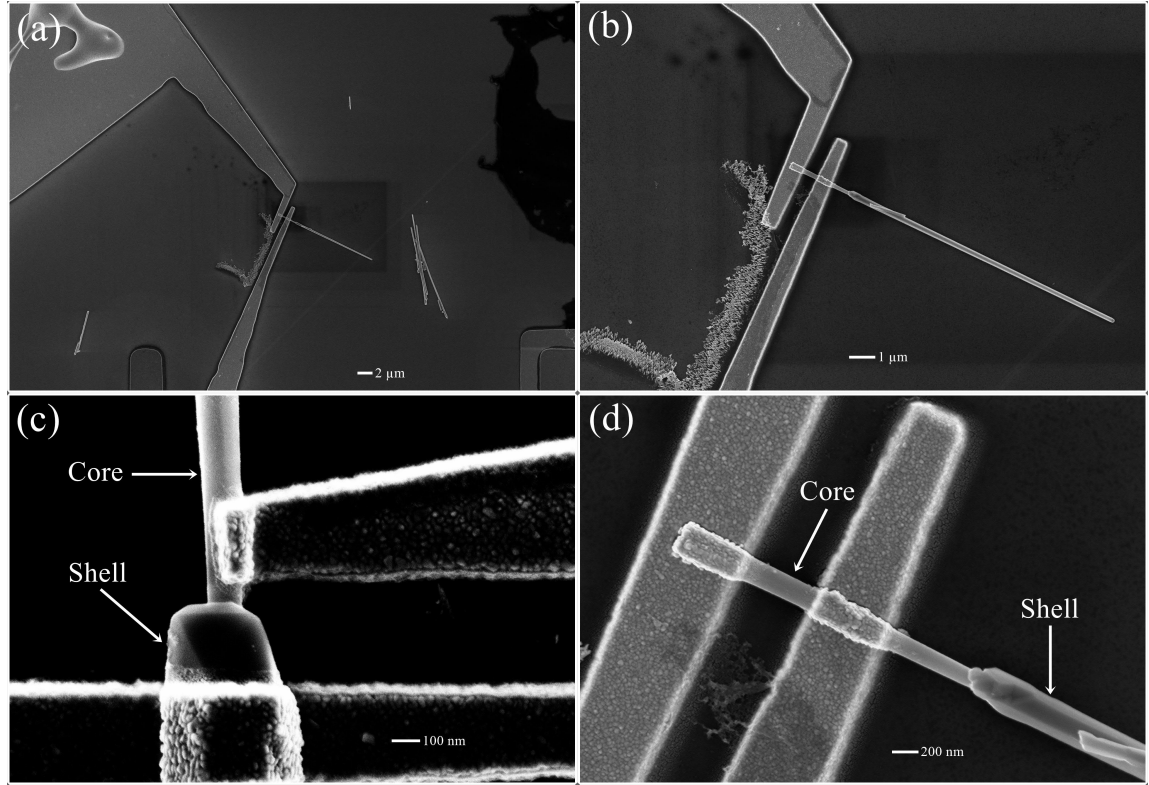
### 5.2.2 EBL layout design



**Figure 5.10:** Part of the layout of the contacts to single nanowire that was designed in LayoutEditor software.

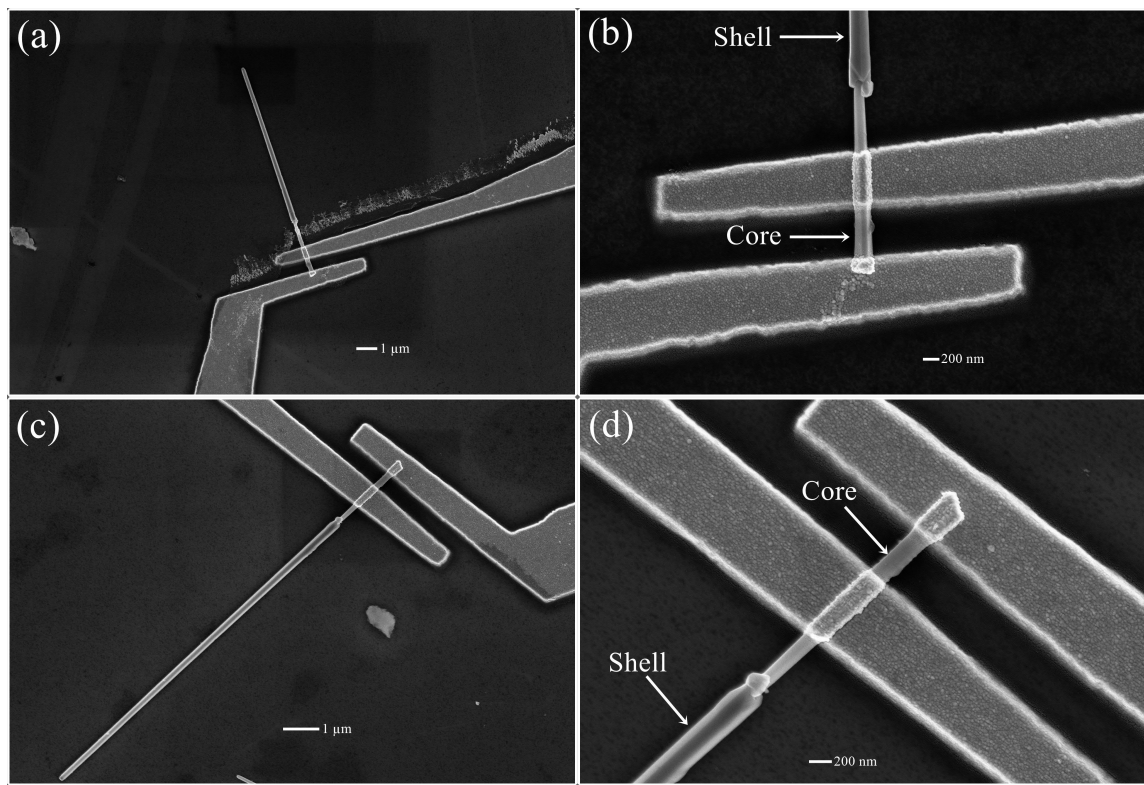
At this point high resolution SEM images were made at different spots of the contact substrate. After that, ImageJ software was used to determine precise coordinates of each NW relative to the lithographically defined grid markers and layout of contacts to single NWs was designed in LayoutEditor software. It is noteworthy that the fact that core and shell had to be connected separately made the whole process more complicated as even the coordinates of the core-shell interface had to be taken into account in order to avoid alignment errors. What is more, the core part of the cs-NW was few times shorter than the shell part which resulted in higher probability of misalignment. Hence, cores were contacted as the first step. Figure 5.10 depicts part of the layout. As can be seen from the figure, there are four pads ( $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$  each) that are connected to single nanowire. Precise location of a single nanowire was set in regards to the alignment markers. Around 20 NWs have been contacted per each chip. BEAMER software environment was used for layout data preparation and its conversion to machine formats readable by EBL apparatus.

### 5.2.3 Electrode contacts to single core-shell nanowires



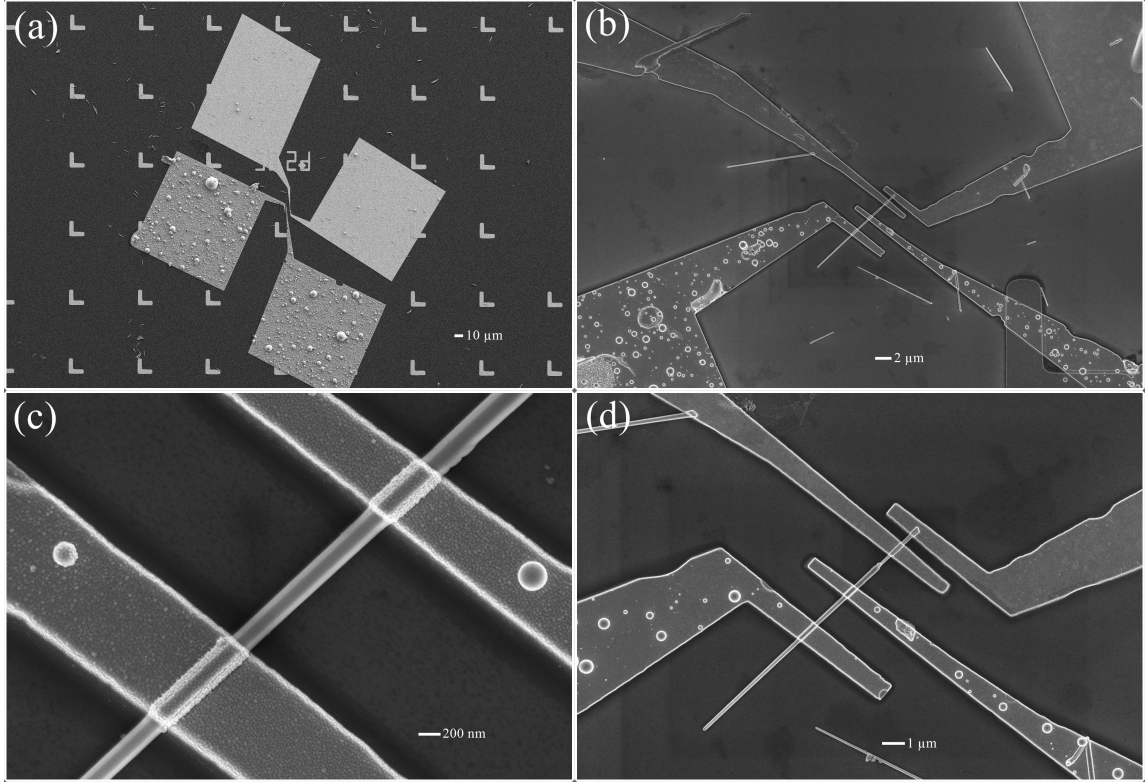
**Figure 5.11:** SEM micrographs of GaAs cs-NWs after EBL exposure, evaporation and lift-off of the core contacts.

Figure 5.11 and figure 5.12 depict metal contacts to the NW cores after the first processing step which consisted of EBL exposure, evaporation and lift-off. As the cores were p-type, an ohmic contact was achieved with  $\text{Au}_{95}\text{Zn}_5$  alloy deposited with evaporation rate of 0.1 nm/s to 0.2 nm/s and total thickness of 115 nm. It is clear from the figures that there was enough clearance for even two contacts to the single core. Close examination by SEM reveals pristine quality metal contacts to the NW body (shown in figure 5.11 (c-d)).



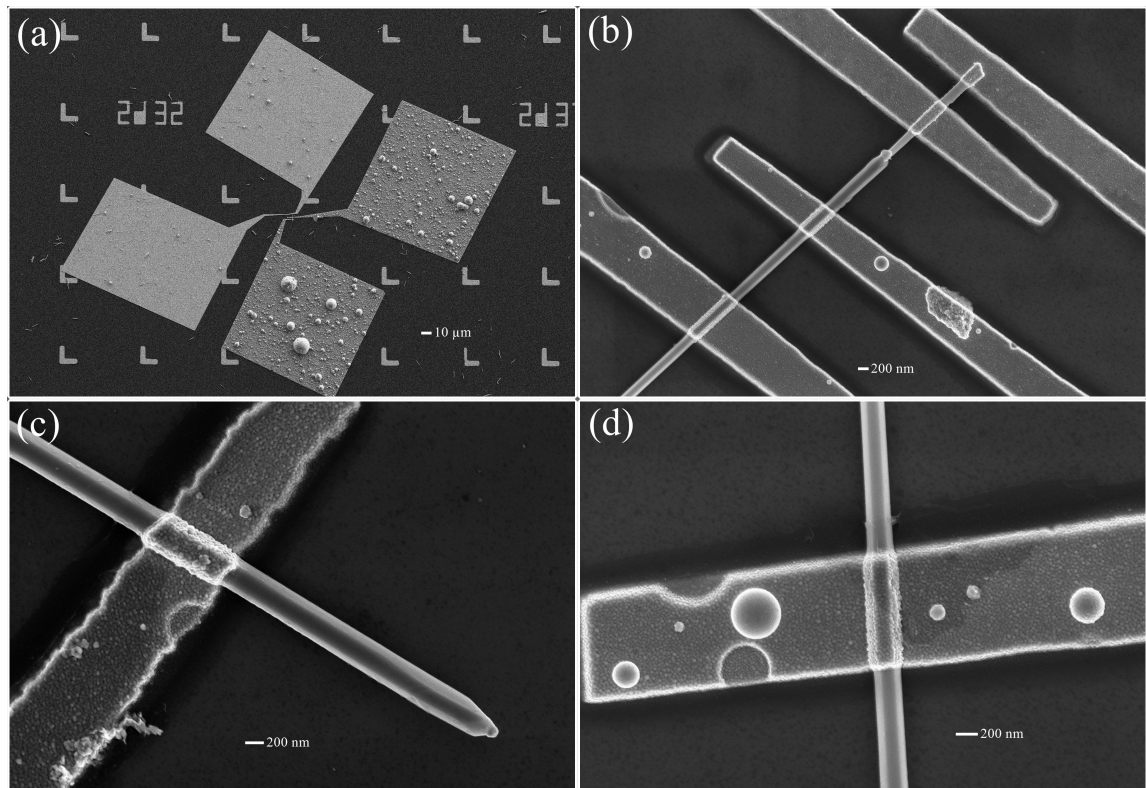
**Figure 5.12:** SEM micrographs of GaAs cs-NWs after EBL exposure, evaporation and lift-off of the core contacts.



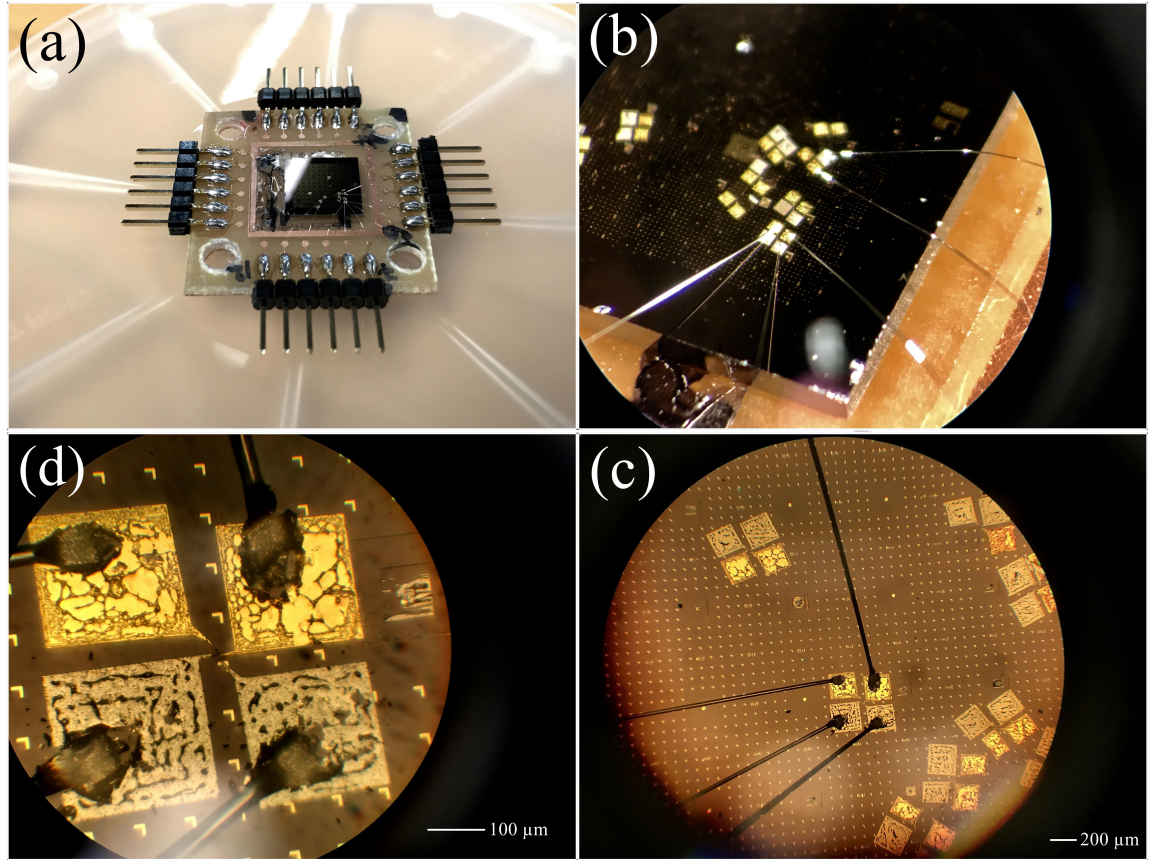


**Figure 5.13:** SEM micrographs of GaAs cs-NWs after EBL exposure, evaporation and lift-off of the core and shell contacts.

Finally, contacts to NW shells were fabricated via the same process described above. Figure 5.13 and figure 5.14 depict metal contacts to the NW shells after the second processing step which consisted of another run of EBL exposure, evaporation and lift-off. As the shells were n-type, an ohmic contact was achieved with Ni/Au<sub>88</sub>Ge<sub>12</sub>/Ni alloy deposited with evaporation rate of 0.1 nm/s to 0.2 nm/s and total thickness of 5 nm/115 nm/15 nm. Rapid thermal annealing tool was utilized to anneal the n-contact metal at 320 °C in N<sub>2</sub> for 60 s. As a result, both electrodes to the cores and to the shell segments of single nanowire were fabricated.



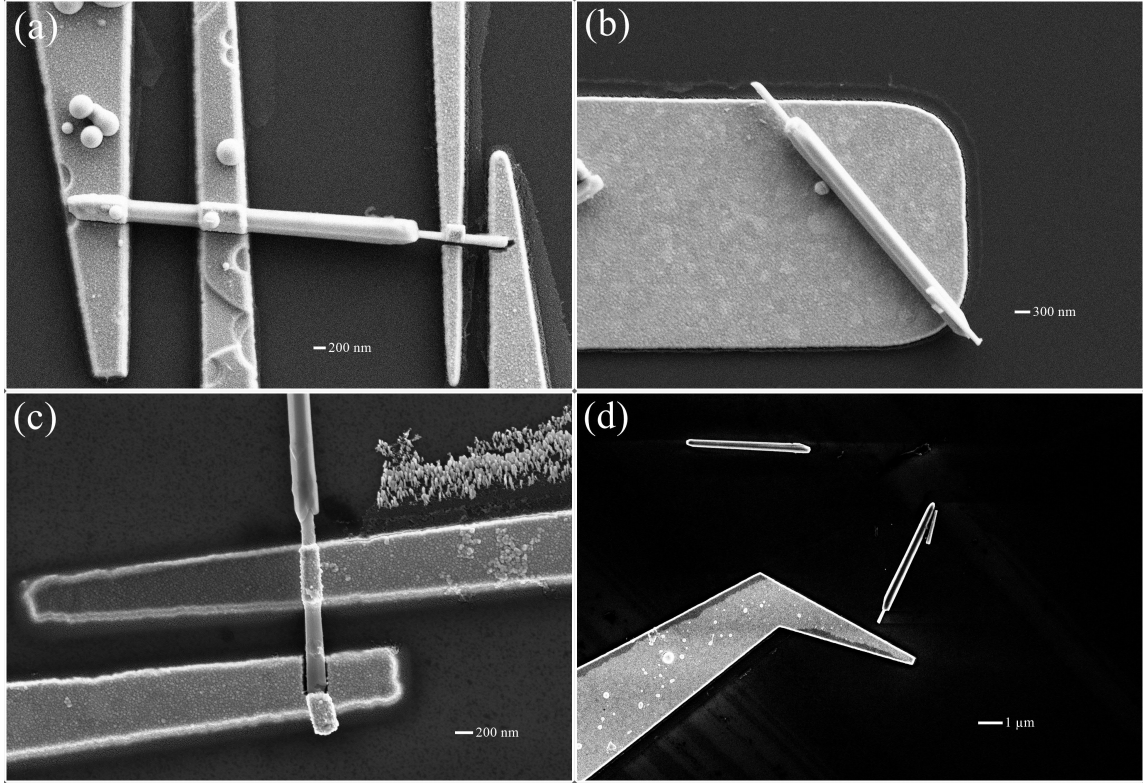
**Figure 5.14:** SEM micrographs of GaAs cs-NWs after EBL exposure, evaporation and lift-off of the core and shell contacts.



**Figure 5.15:** Prototype photovoltaic device that consists of several single nanowire solar cells on one chip. Bonding was used to connect NW pads to external pins.

Lastly, a photovoltaic device was fabricated. In order to connect each single nanowire solar cell to the outside world, custom printed circuit board was used. The chip with several single nanowire solar cells was fixed to the board and manual thin wire bonder was used to bond each pad to external pin connectors. Figure 5.15 presents images of the final device and bonded pads at different magnifications. As a result, a single chip and therefore every single nanowire on it can be connected to almost any external apparatus or even used in embedded systems.

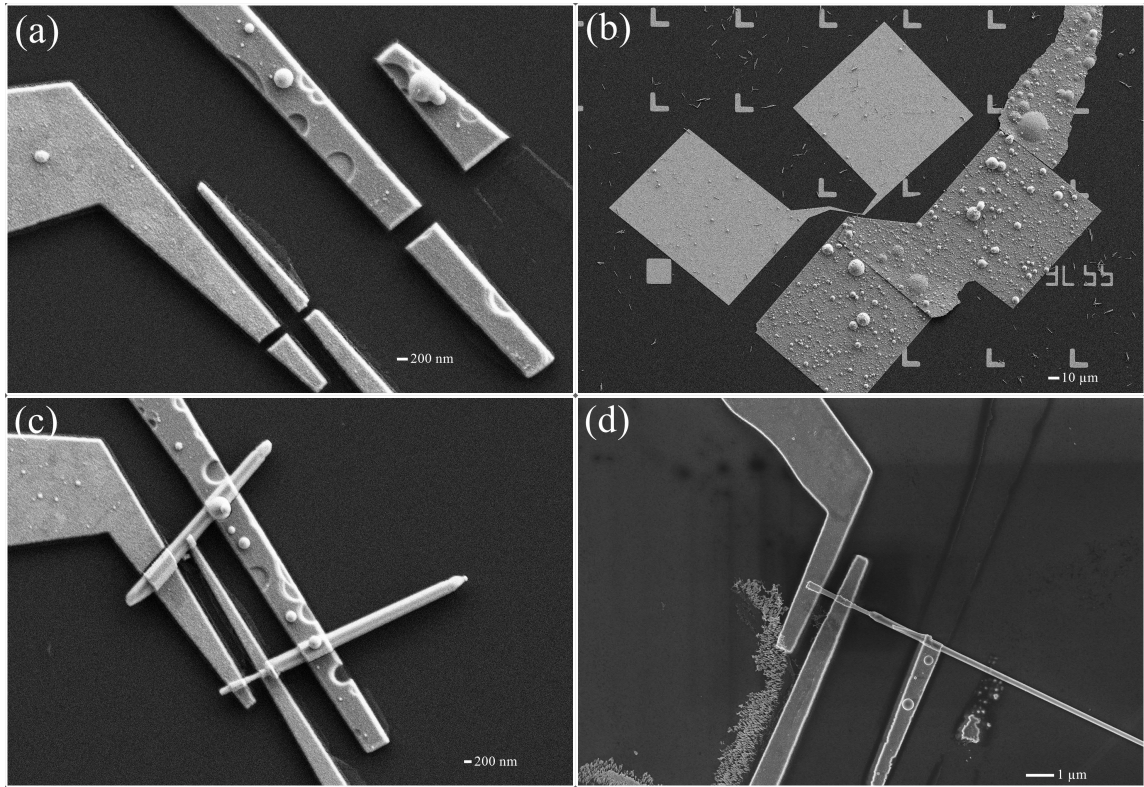
### 5.2.4 Fabrication challenges



**Figure 5.16:** SEM micrographs of typical problems that were encountered during single nanowire contacting.

A number of different fabrication problems arose during creation of single nanowire solar cells. Figure 5.16 and figure 5.17 depict some of the prevalent difficulties that were encountered during single nanowire contacting. Perhaps most demanding were evaporation and lift-off. In particular, thick nanowire side walls acted as shadow mask resulting in metal gaps, effectively breaking the contact pad connection (shown in figure 5.16 (a)). Even though the problem was resolved by tuning the total diameter of NWs, sometimes it was troublesome to properly contact the core (figure 5.16 (c)) because it actually floated in the air due to the fact that shell is much thicker (clearly visible in figure 5.16 (b)). One notable solution would be to apply an additional polymer spacer layer with the thickness equal to the radius of a single nanowire that would eliminate the shadow effect of NW side walls [120]. Moreover, the rapid thermal annealing step after the evaporation and lift off resulted

in better contact possibly due to the melting of the metal and consequent elimination of the metal gaps. Another obvious problem was misalignment (presented in figure 5.16 (d)) which was highly dependent on the quality of the SEM images.



**Figure 5.17:** SEM micrographs of typical problems that were encountered during single nanowire contacting.

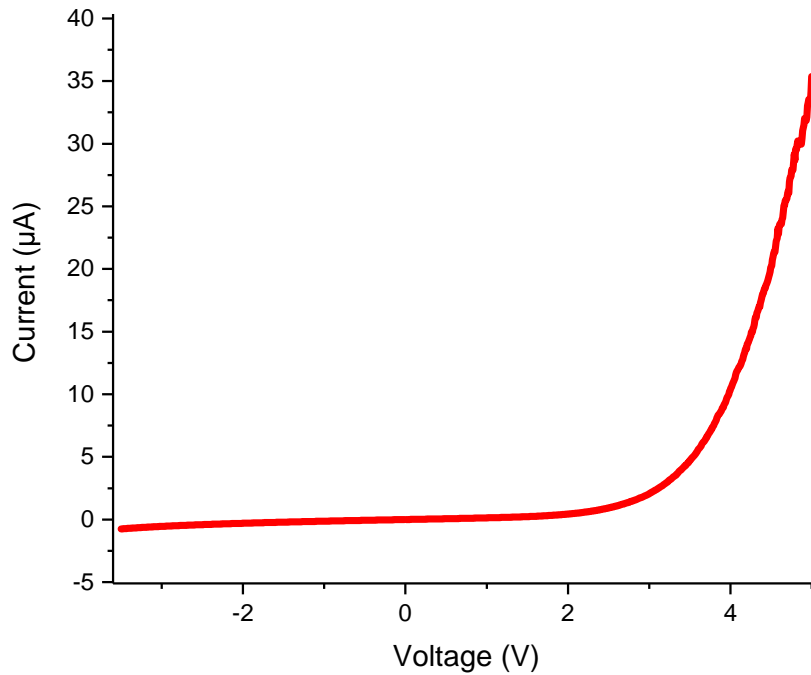
Furthermore, a common problem was the displacement of the NWs during the contacting process. As an example, figure 5.17 (a) shows gaps that were left after the NW was displaced and figure 5.17 (c) depicts a situation when another NW changed its position and blocked the contacts completely. The problem was solved by avoiding the use of nitrogen drying gun after each lift-off or developing step and letting the liquid dry itself. What is more, retention, a typical issue associated with lift-off, was a recurring problem especially for the shell Ni/Au<sub>88</sub>Ge<sub>12</sub>/Ni metal stack (shown in figure 5.17 (b)). Additionally, some contacts were completely removed with the sacrificial layer as can be seen in figure 5.17 (d).



## 5.3 Electrical and optical properties

### 5.3.1 Unpassivated core-shell GaAs nanowires

The current-voltage (I-V) characteristics of the GaAs single nanowire solar cells were obtained using Karl Süss Probe station equipped with HP 4155A semiconductor parameter analyzer. Figure 5.18 presents I-V curve measured from a single unpassivated cs-NW in the dark. We observed perfect diode's behaviour with current flows in micro ampere range and threshold voltage at about 3 V. The junction I-V characteristic are non-linear and asymmetric with the reverse leakage current ranging from 100 pA to 750 pA at  $-1$  V to  $-3.5$  V respectively. There is an exponential increase in current at low voltage and ohmic behaviour above the turn-on voltage. Thus, a p-n junction was successfully formed.



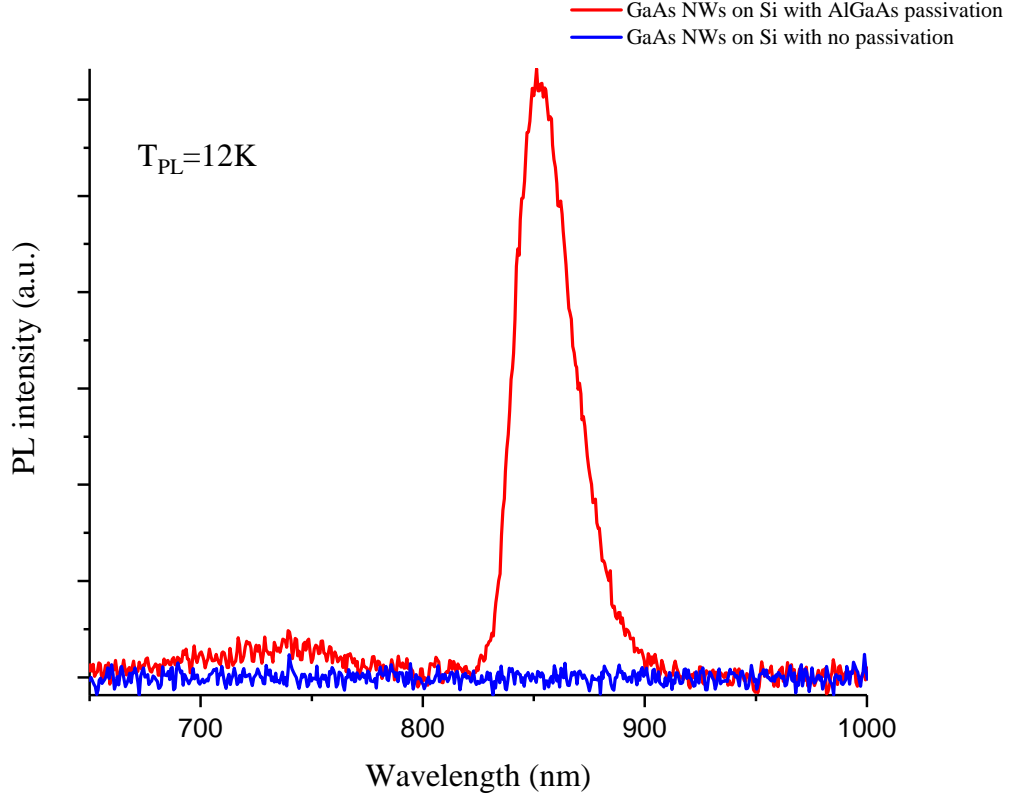
**Figure 5.18:** Dark I-V characteristics of the unpassivated GaAs single nanowire solar cell.

However, no photo response was observed during I-V measurements under

illumination. We attribute this to the surface effects present in unpassivated GaAs NWs that severely limit the performance and degrade device characteristics by pinning the surface Fermi energy. Therefore, in situ passivation had to be considered.

### 5.3.2 AlGaAs passivation of core-shell nanowires

As was discussed in section 3.3, AlGaAs epitaxial passivation can eliminate the surface states and prevent the carriers from recombining non-radiatively. For this reason, a study of AlGaAs passivation effect on optical and electrical properties of core-shell GaAs NWs was performed. The PL measurements of GaAs cs-NWs on GaAs substrates are not feasible as the emission from the substrate overlaps any peaks from the actual NWs. Hence, separate samples with GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$  cs-NWs were grown on Si (111) substrates. The 40 nm diameter Au NPs were used as catalyst. The initial growth temperature was 470 °C and the nominal V/III ratio during the cores growth was 25. Next, the temperature was increased to 650 °C for the radial growth of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  shells. The molar ratio  $X_{\text{As}}/X_{\text{Ga}} + X_{\text{Al}}$  during the passivation was set to 30. Figure 5.19 shows 12 K PL spectra of unpassivated GaAs NWs grown on Si substrate and GaAs NWs with AlGaAs passivation grown on Si substrate with exactly the same parameters.



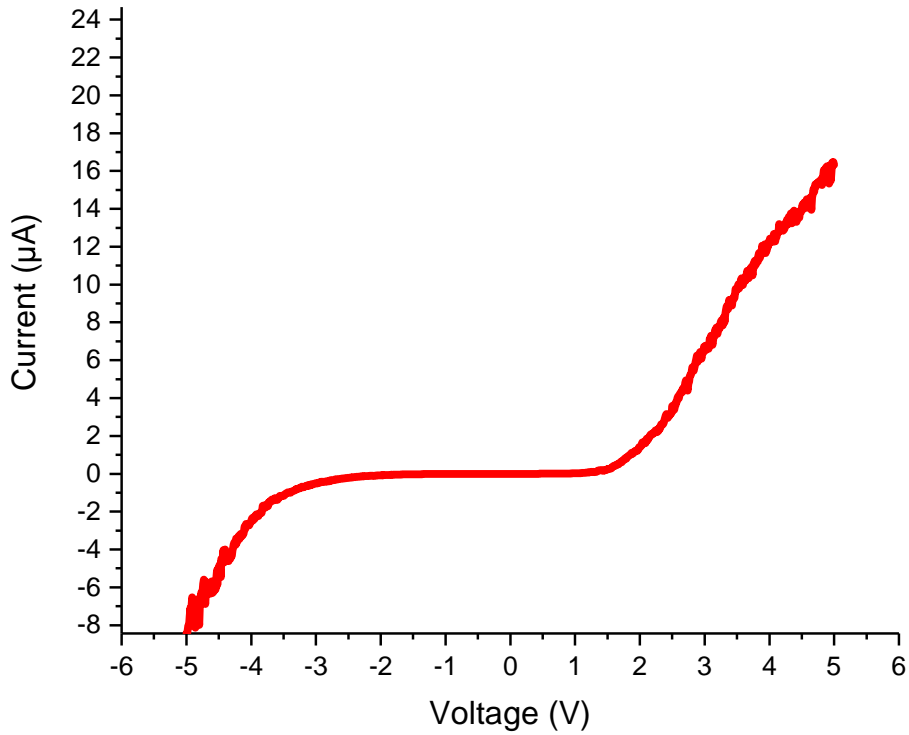
**Figure 5.19:** LT PL spectra measured at 12K for GaAs NWs on Si substrate with and without AlGaAs passivation. The spectrum of GaAs NWs is shown in blue and the spectrum GaAs/AlGaAs cs-NWs is depicted in red. A dramatic enhancement of PL intensity was observed for the same NWs with AlGaAs passivation.

It is clear from the figure, that unpassivated GaAs NWs grown on Si substrate in our MOVPE apparatus did not show any signal at low temperature measurements. Furthermore, even fivefold increase of the laser power did not reveal any emission from the samples. This is due to high density of surface states and surface depletion effect. However, AlGaAs shell passivation resulted in strong PL signal with the peak position at 851 nm. This corresponds to 1.45 eV and it is in good agreement with the previous studies [43, 47]. Hence, AlGaAs passivation effectively resolves GaAs inherited problems associated with surface recombination.



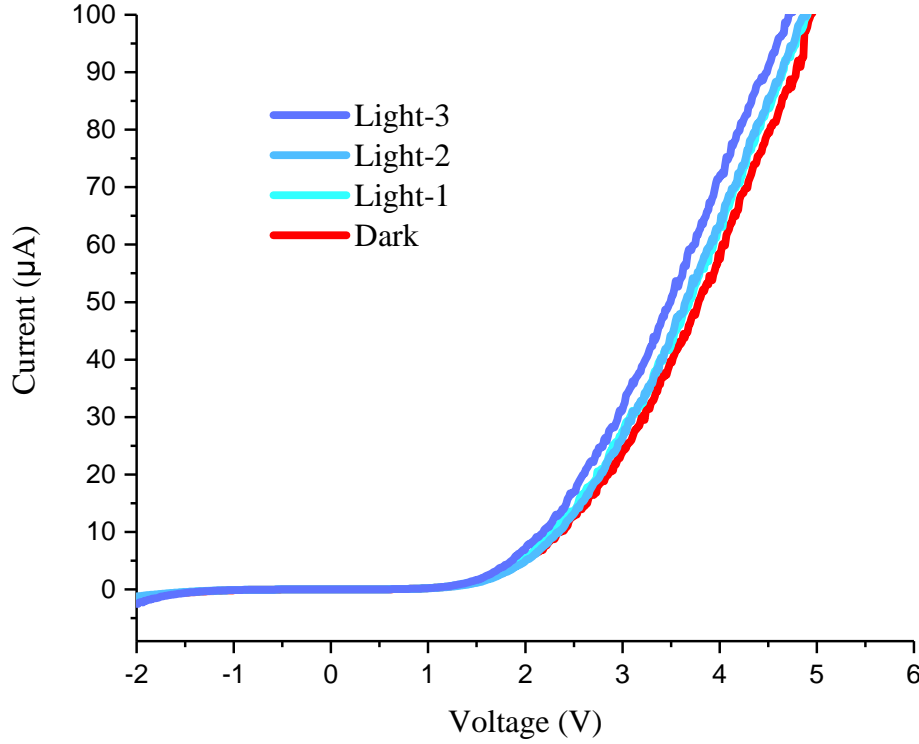
### 5.3.3 Single nanowire photovoltaic device

Consequently, additional 5 s AlGaAs passivation step was added to cs-NW recipe and the new series of single nanowire solar cell samples has been prepared. Figure 5.20 shows the full dark I-V characteristics of the single cs-NW passivated in situ with AlGaAs.



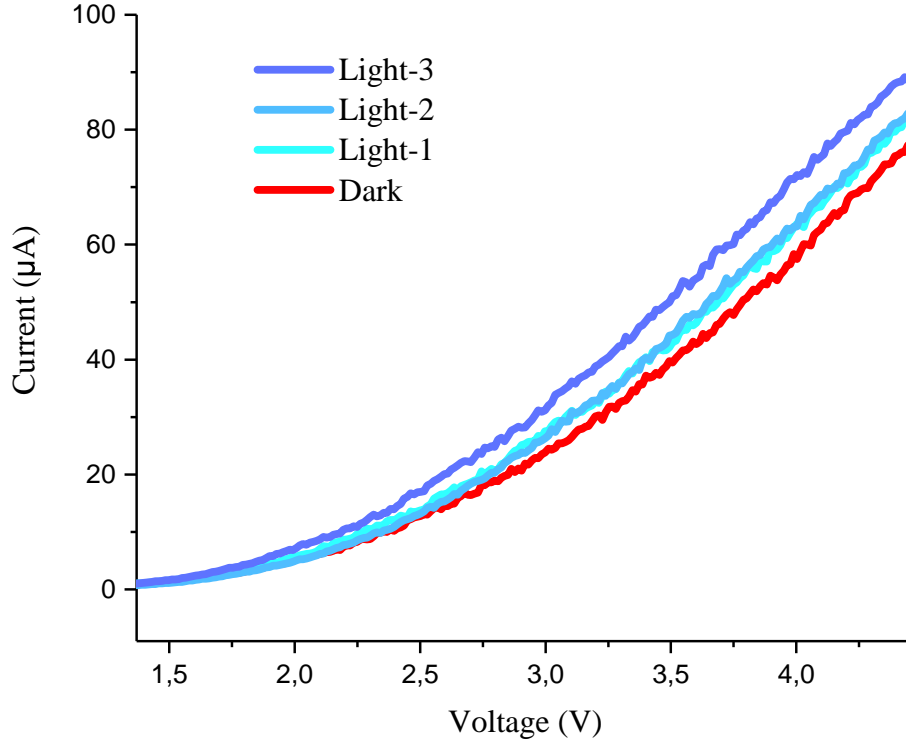
**Figure 5.20:** I-V characteristics of the AlGaAs passivated GaAs single nanowire.

The single cs-NW fabricated by shell-substrate isolation technique showed clear rectifying behaviour with forward bias threshold voltage at about 2 V and break-down voltage at roughly  $-4$  V. The reverse leakage current was found to be from 5 pA to 490 pA at  $-1$  V to  $-3$  V respectively. Figure 5.21 depicts I-V characteristics of the AlGaAs passivated GaAs single nanowire device both in the dark and under increasing light illumination.



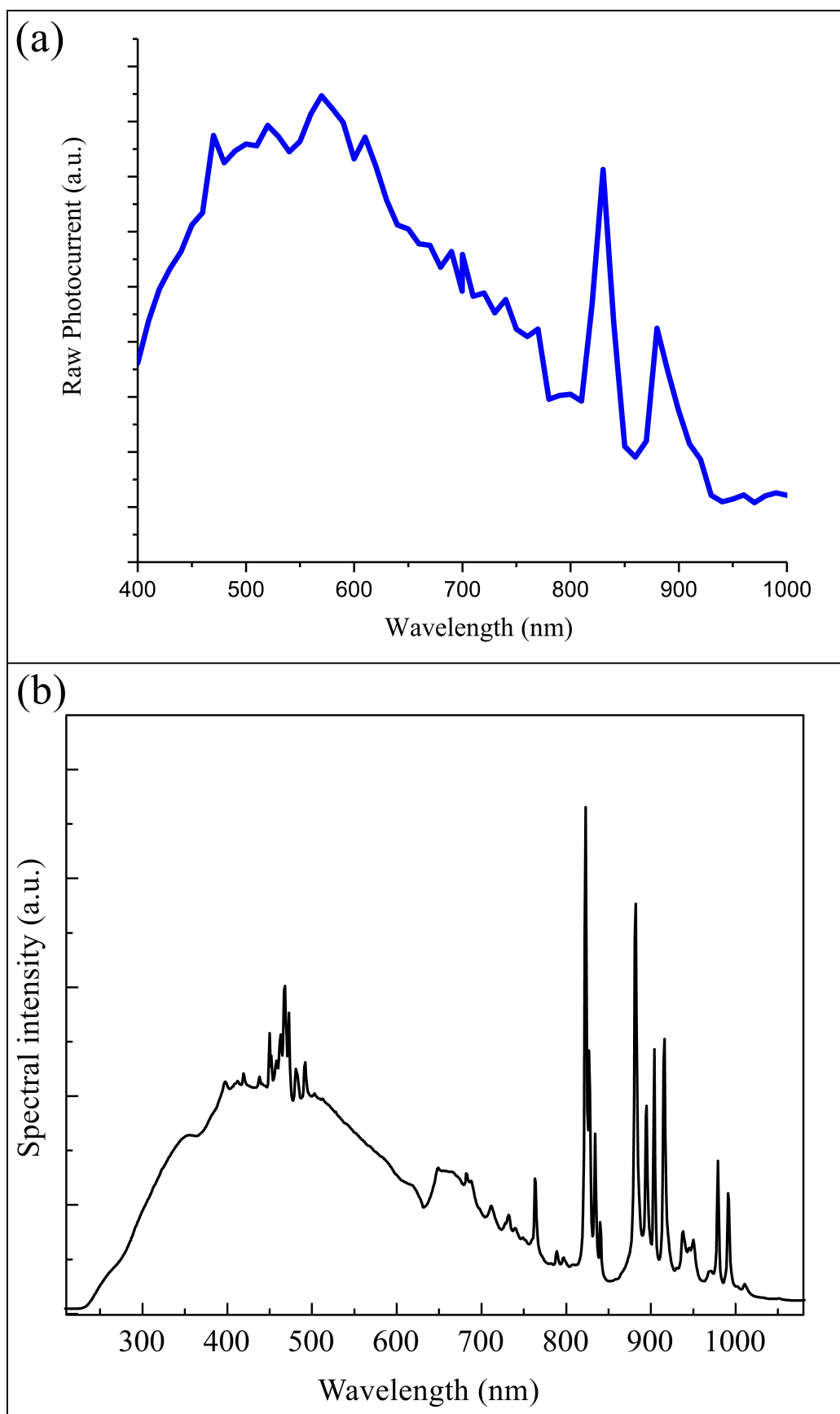
**Figure 5.21:** I-V characteristics of the AlGaAs passivated GaAs single nanowire device. Different colours represent measurements in the dark and under increasing illumination intensity.

Looking at the figure, we can clearly see that there is a steady increase of current due to electron-hole pairs generation as a result of increasing light intensity. Figure 5.22 shows higher magnification segment of the same measurement. On average, there is a  $15 \mu\text{A}$  increase in the junction current due to photocurrent contribution. Although the current values may seem low, it is noteworthy that the presented curves are the measurement of single nanowires. Apparently, once there are hundreds of millions of NWs on one substrate, a significant increase of photocurrent is expected as each and every NW would act as photovoltaic element.



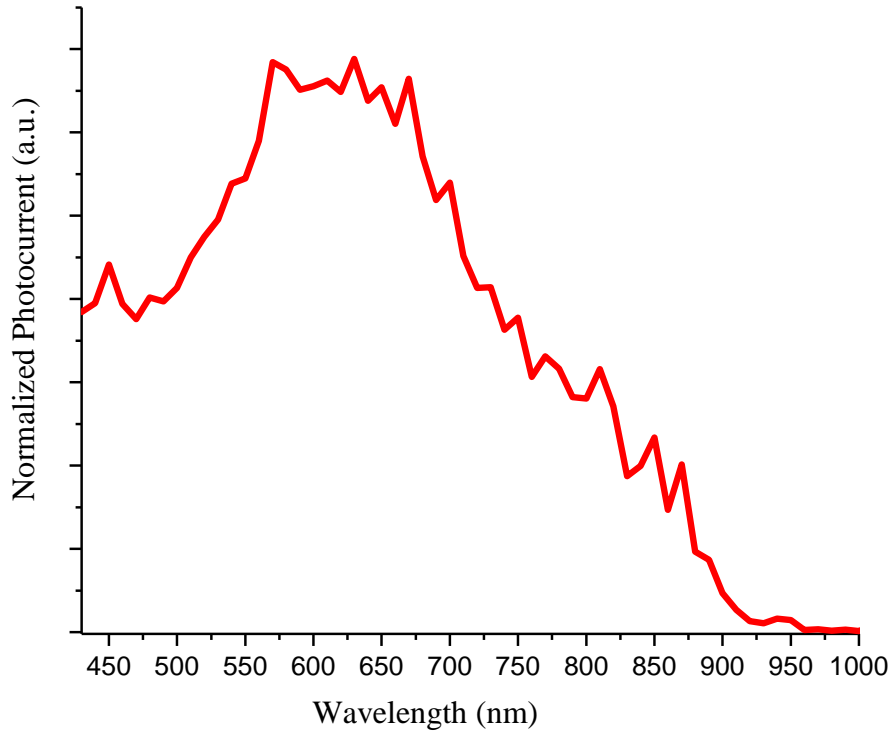
**Figure 5.22:** I-V characteristics of the AlGaAs passivated GaAs single nanowire device. Different colours represent measurements in the dark and under increasing illumination intensity.

To further investigate the optical properties, wavelength dependent photocurrent measurements were conducted using the setup described in section 4.7. Figure 5.23 (a) depicts the raw photocurrent signal without normalization measured at an applied bias of 3.5 V at room temperature. The raw spectrum is actually a product of several elements such as diffraction gratings efficiency, transmission of optics and detector sensitivity. Obviously, the main light source, xenon arc lamp, is the biggest contributor to the raw spectrum response of the single nanowire. Remarkably the photocurrent spectrum precisely follows the xenon arc lamp emission spectrum which depicted in figure 5.23 (b). By comparing the two figures we can clearly see the same peaks at roughly 475 nm, 830 nm and 890 nm. Apparently, we can identify the fabricated single nanowire device as a photodetector.



**Figure 5.23:** (a) Raw photocurrent spectrum of the single nanowire photodetector at 3.5 V bias at RT. The incident light power varied mainly due to the lamp spectrum. (b) Xenon arc lamp emission spectrum (public domain).

In order to see the actual spectral response of the nanoscale photodetector, power normalized measurements were performed. Figure 5.24 presents photocurrent spectrum normalized to the power of incident light at 3.5 V bias and room temperature. In fact, power normalized photocurrent measurements represent the responsivity of the single nanowire photodetector. However, the values are arbitrary because a number of variables, such as the exact power density at the detector, the precise exposed area of the NW device and the power at the pyroelectric detector, were unknown.



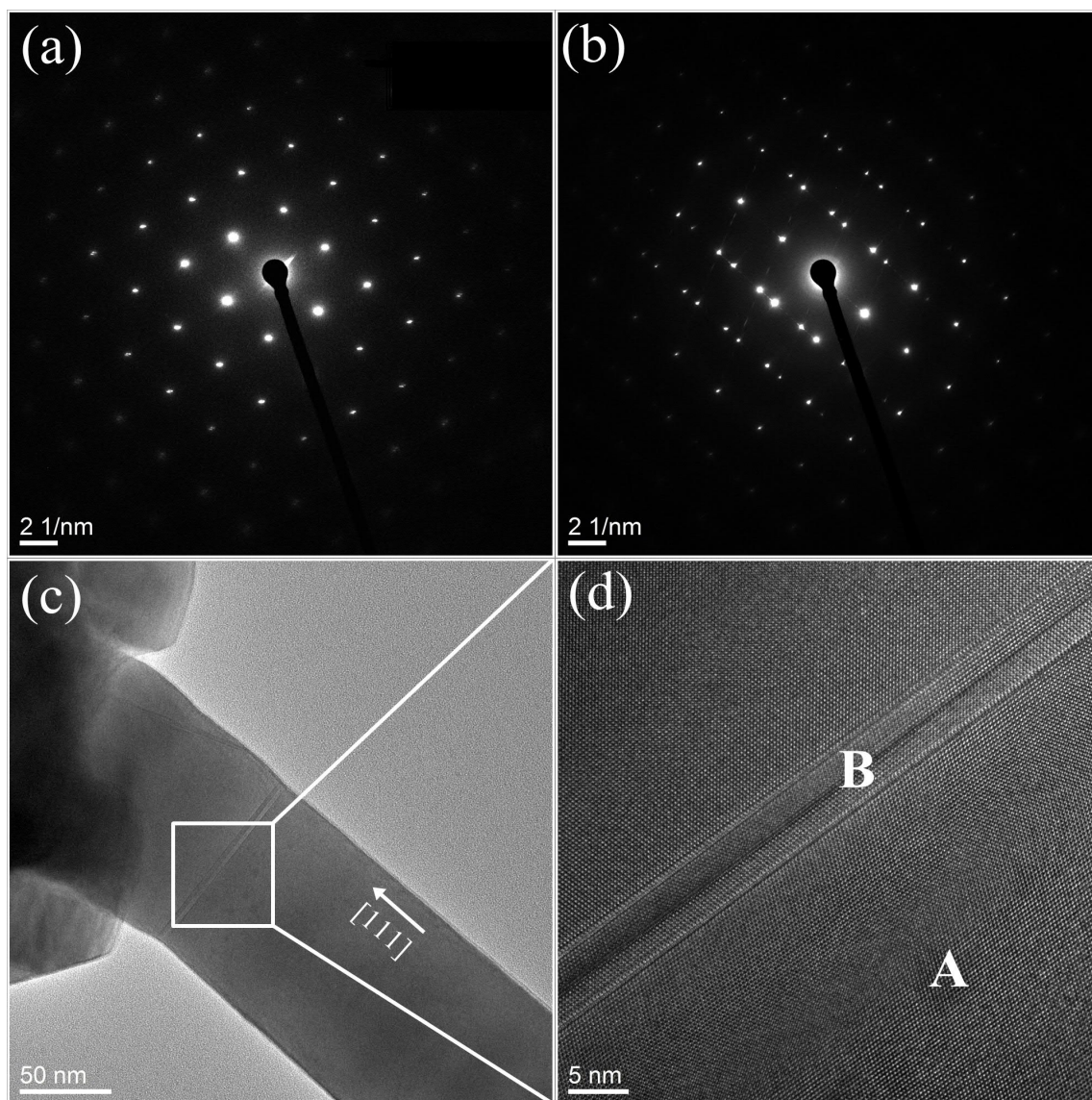
**Figure 5.24:** Photocurrent normalized to the power of incident light at 3.5 V bias at RT. The curve actually represents the responsivity of the single nanowire photodetector expressed in arbitrary units.

The fabricated single nanowire photodetector exhibits a broad spectral response in the 450 nm to 800 nm (visible spectrum) range with the distinct peak at about 650 nm which corresponds to the band gap of the AlGaAs composition used in this work. This demonstrates the high purity and the

superior crystal quality of the grown NWs which was also confirmed by TEM. The different photocurrent peaks are linked to the polarization and incident angle of the light and, most importantly, specific surface optical modes of a single nanowire that are determined by its geometry. In fact such modes may be used to further enhance and tune the fundamental absorption properties of NWs [121]. However, the study of those is out of the scope of this work.

## 5.4 Crystal structure of the core-shell nanowire device

Crystal structure of unpassivated GaAs cs-NWs was investigated with TEM. Figure 5.25 (c) presents TEM micrographs of the NW core. As expected for epitaxial NW growth on (111) substrates, the growth direction was identified as  $[111]$ . Figure 5.25 (d) shows a segment of the core with a twin plane, diffraction patterns outside the twin plane (a) and at the twin plane (b). Predictably, the diffraction pattern corresponds to zinc blende crystal structure. The location of the dislocation defines the start of the core regrowth.

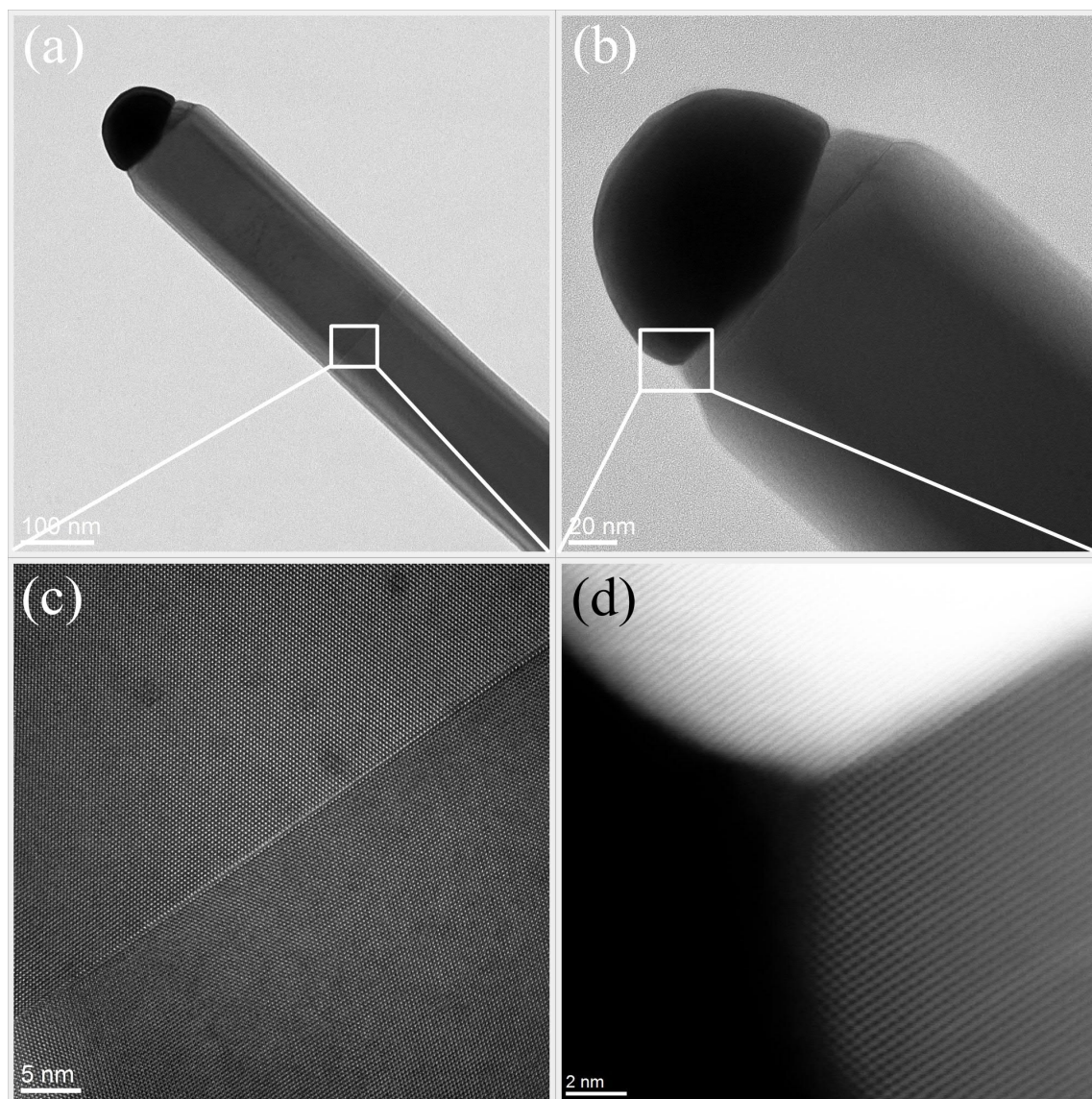


**Figure 5.25:** (a) TEM micrograph of the NW core. The growth direction was identified as  $[111]$ . The segment of the core with a twin plane (d) and diffraction patterns outside the twin plane (spot A) (a) and at the twin plane (spot B) (b). The diffraction patterns correspond to zinc blende crystal structure. The location of the dislocation defines the start of the core regrowth.

Figure 5.26 (a-b) shows TEM micrographs of the segment with Au tip and nanowire shell. Figure 5.26 (c) reveals almost pristine quality crystal



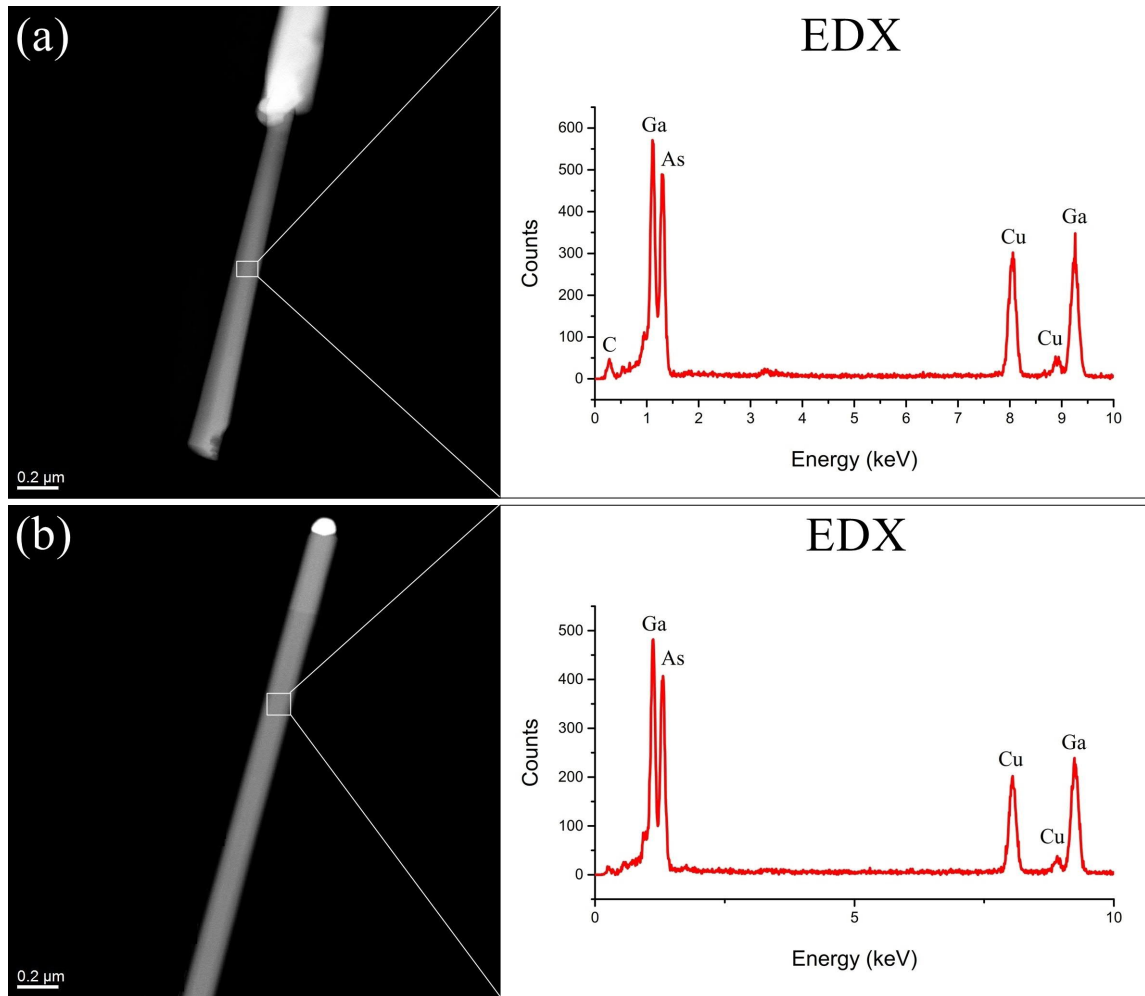
structure with only one twin plane along the whole shell length. Figure 5.26 (d) depicts sharp interface between GaAs and Au tip indicating that there are no intermediate compounds and Au operates as a VLS catalyst.



**Figure 5.26:** (a) TEM micrograph of the NW shell and its magnification image (c) reveal almost pristine quality crystal structure with only one twin plane along the whole shell length. The segment with Au tip and nanowire shell (b) depicts sharp interface between GaAs and Au tip (d) indicating that there are no intermediate compounds and Au operates as a VLS catalyst.



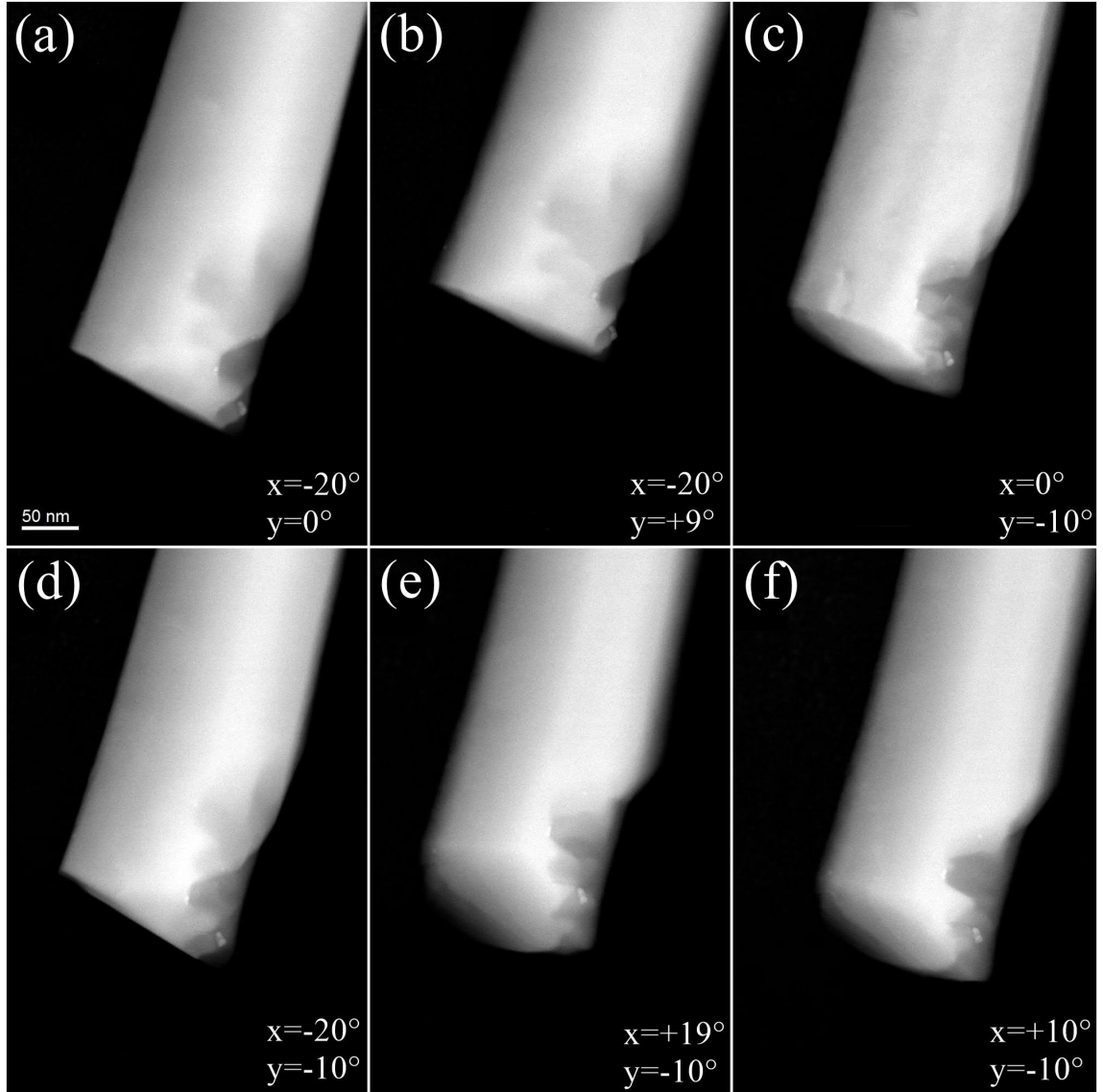
EDX analysis was performed for chemical characterization of NWs. Figure 5.27 depicts EDX spectra taken from the shell (a) and from the core segments (b). The data confirms strong presence of Ga and As which unambiguously shows that the prepared nanowires are GaAs. Elemental analysis showed no significant composition of Zn and Si dopants which indicates the dopant concentration of less than one percent. However, as the EDX accuracy range is on the order of one atomic percent, naturally, the dopant concentrations are much lower than that. Copper and carbon peaks originate from the TEM copper grids covered with a holey carbon film.



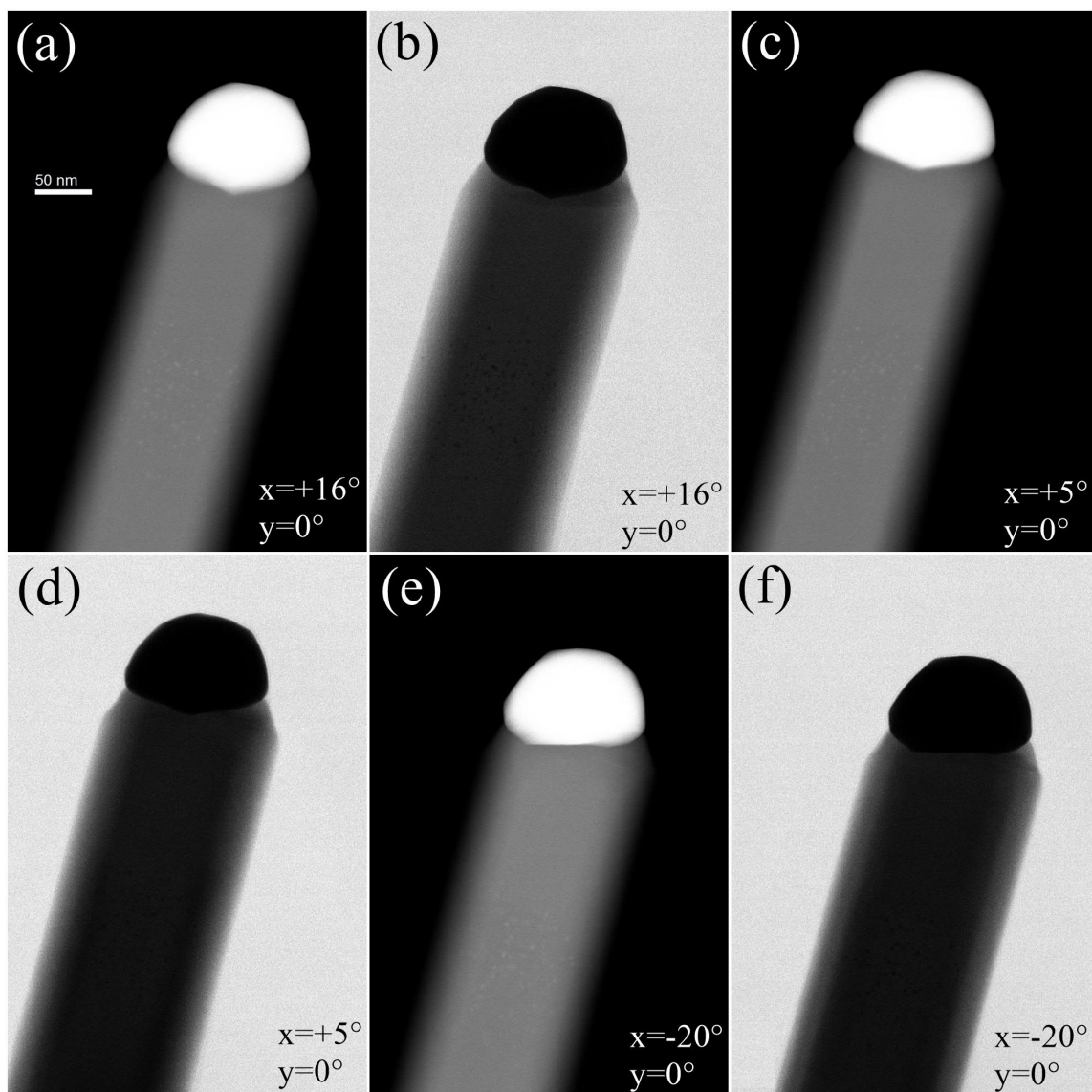
**Figure 5.27:** EDX spectra of the shell (a) and the core segments (b). Strong presence of Ga and As confirms that the prepared nanowires are GaAs. No significant composition of Zn and Si dopants was detected due to low accuracy range of the EDX that is insufficient to identify the dopant concentrations on ppm level. Copper and carbon peaks originate from the TEM copper grids covered with a holey carbon film.

One interesting phenomenon that we observed was nearly cylindrical shape of the core segment. Although NW tip was clearly hexagonal (as shown in figure 5.1 (d)), it was difficult to see the facets of the core in SEM. In order to investigate it further, TEM micrographs of the core at different tilt angles were obtained (figure 5.28 (a-f)). It is clear that core exhibits almost cylindrical shape though generally it is expected to be hexagonal.

Reasons for this are unclear, but cylindrical NWs have been also reported in other studies [122, 123]. Similar scans at different tilt angles were carried out for the shell segment (figure 5.29 (a-f)). TEM images reveal presence of the facets and confirm that shape of the shell is indeed hexagonal.



**Figure 5.28:** (a-f) TEM micrographs of the nanowire core at different tilt angles that indicate its nearly cylindrical shape.



**Figure 5.29:** (a-f) Both dark-field and bright-field TEM micrographs of the nanowire shell at different tilt angles that indicate its hexagonal shape.

## Chapter 6

# Conclusions

The aim of this work was to fabricate and study the fundamental working mechanisms of single nanowire solar cell and photodetector based on novel radial p-n junction in a core-shell geometry. The Au-assisted core-shell GaAs NWs were grown on GaAs(111)B substrates with an atmospheric pressure metalorganic vapour phase epitaxy. Group III trimethylgallium (TMGa) and group V tertiarybutylarsine (TBAs) were used as sources of gallium (Ga) and arsenic (As) while diethylzinc (DEZn) and disilane ( $\text{Si}_2\text{H}_6$ ) were used for p-type and n-type doping of NWs respectively.

In this study, a unique lithography-free technique was employed on an ensemble of NWs to isolate the core (p-type) from the shell (n-type) on the growth substrate. The method employed the two-step growth process interrupted by application of the insulating spin-on glass layer. The core-shell NWs with typically 150 nm diameters and several micrometres length were then transferred mechanically onto an insulating substrate. Electron beam lithography was used to make metal contacts to single core-shell NWs. Specific contact schemes were used to obtain an ohmic contact between the metal electrodes and NW cores and shells.

The crystal structure of core-shell GaAs NWs was examined with high-resolution transmission electron microscopy. The NWs crystallized in the zinc blende crystal structure and exhibited excellent crystallographic properties and low defect density. In fact, TEM revealed almost pristine quality crystal structure with only one twin plane along the whole shell length which verified that the whole structure comprised single crystal and no other defects occurred as result of the regrowth process. Energy-dispersive X-ray spectroscopy confirmed strong presence of Ga and As which unambiguously showed that the prepared NWs were indeed GaAs. Morphological properties of the NWs used in this work were inspected using scanning electron microscopy.

The optical and electrical characterization of fabricated single nanowire devices was performed. The I-V characteristics showed perfect rectifying diode's behaviour, which proved the feasibility of the isolation method. However, no photo response was observed from unpassivated NWs due to high density of surface states. Surface passivation of NWs was identified as one of the key issues in functioning of the photovoltaic device and a study of AlGaAs passivation effect on optical and electrical properties of core-shell GaAs NWs was performed. In particular, a dramatic enhancement of PL intensity was observed for the AlGaAs passivated NWs. The I-V measurements of AlGaAs passivated single nanowire devices revealed a steady increase of current due to electron-hole pairs generation as a result of increasing light intensity. What is more, the photocurrent measurements showed broad spectral response in the 450 nm to 800 nm (visible spectrum) range, indicating a successful working of a single nanowire as a photodetector. Finally, an attempt was made to build a prototype photovoltaic device that consisted of several single nanowire devices on one chip

Although a working radial p-n junction was demonstrated, no solar response was detected from the single nanowire structure because of yet many challenges that have to be addressed in order to obtain a fully functional single nanowire solar cell. First, a nominally intrinsic region should be considered as it will increase the absorber area and reduce the interfacial recombination of radial p-n junction. Next, the metal-semiconductor junction can be further optimized to achieve better ohmic contact and minimize the contact resistance. It is crucial to fine-tune the physical contact between electrode and NW as it remains a dominant problem. Further investigation is also needed on the photo response under various conditions such as different bias voltage, light polarization and temperature. Once the above-mentioned optimizations for single nanowire device are carried out, the demonstrated fabrication process can be used for making progress towards realising the functional single nanowire based radial p-n junction solar cells in the future.

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